WAVECREST Corporation

Jitter Analysis 101

A Foundation for Jitter Measurements

209000-07 REV A

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U.S. Patent Nos. 4,908,784 and 6,185,509 and 6,194,925; other United States and foreign patents pending

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Jitter Analysis 101

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Fundamentals of Jitter Analysis

Intro to Jitter Testing

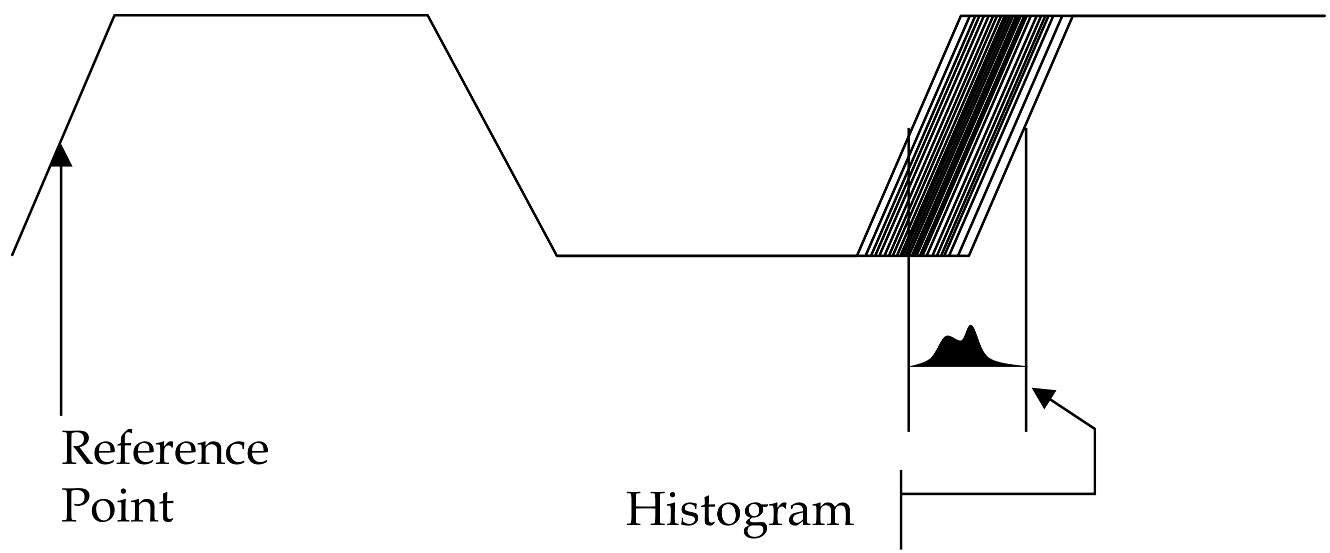
- Why test for Jitter?
  - Device Speeds are exceeding 1GHz
    - Setup time budgets getting tighter thereby reducing total jitter budget
  - Studies show a clear link between jitter and overall device performance and BER
    - For Serial Communications Device Manufacturers, Jitter Testing is faster and more conclusive than production bit error rate testing
      - Fibre Channel specifications call for 14 σ reliability. This would take over 15 minutes to test using a BERT while less than 1 second using jitter techniques.
  - Jitter is the final frontier for high speed logic
    - Today's simulation software virtually guarantees functionality but cannot accurately estimate jitter performance
    - Once functionality has been established, overall performance optimization is the next step
  - Jitter can identify process variations.
    - Certain jitter components are sensitive to impurities, thermal variations and cross talk (cross talk may indicate poor signal separation.)
- Bottom line...Jitter performance of a circuit translates to overall system performance.

What is Jitter?

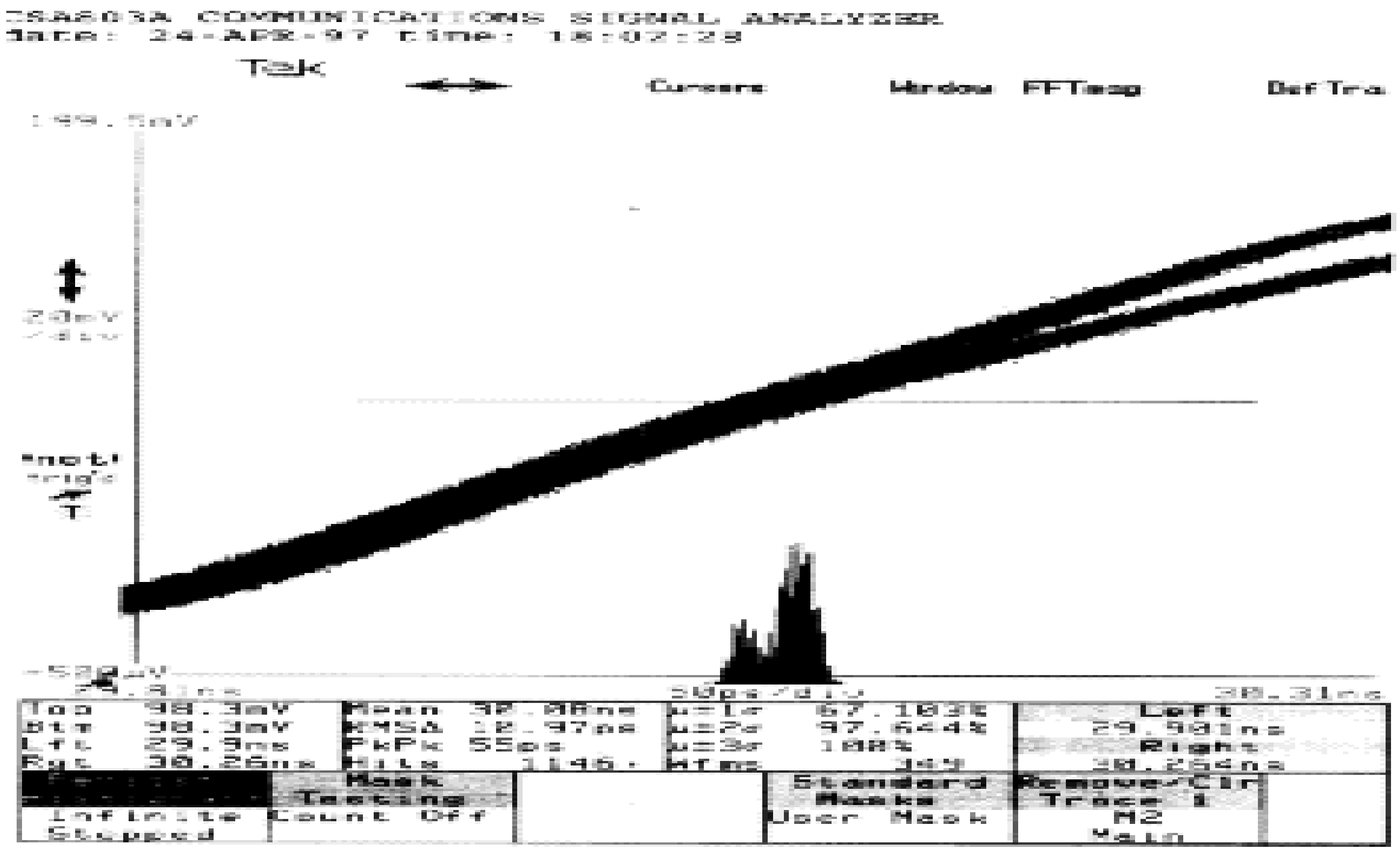
- Jitter -

  "The deviation from the ideal timing of an event. ... Jitter is composed of both deterministic and Gaussian (random) content."

  T11.2 / Project 1230/ Rev 10 Fibre Channel - Methodologies for Jitter Specification page 7.

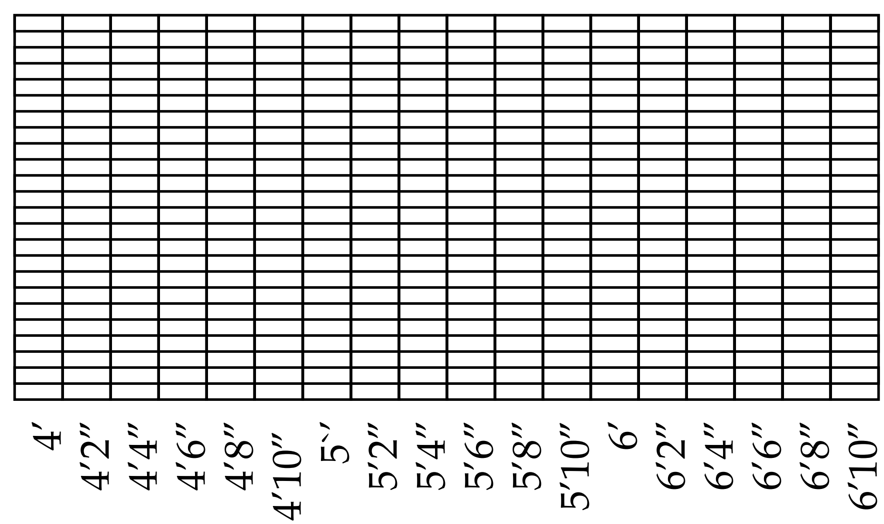


Using a Sampling Oscilloscope



What is a Histogram?

- A Histogram is:
  - A two dimensional plot of the distribution of measurements
    - Each point on the Histogram answers the question: How many measurements had X for a measurement?
  - Compares measurements or data points to the number of occurrences of that particular measurement or data point.
  - A catalog of all measurements made organized by value of measurement.
- An Example
  - Attendees Height



What is Jitter Made of?

Why does it occur?

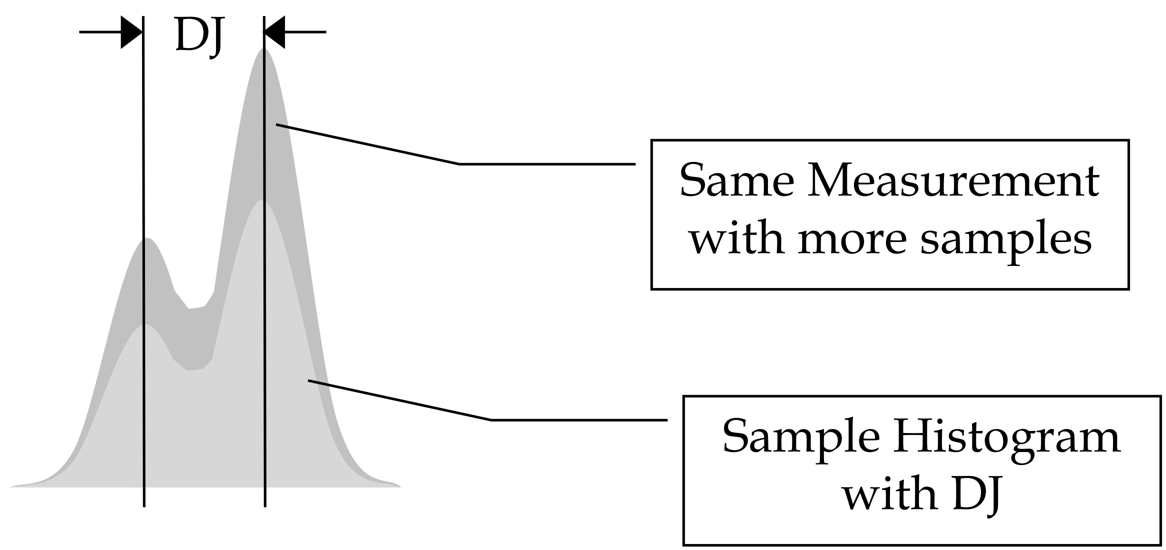
How will it effect my circuit?

What is Jitter Composed of?

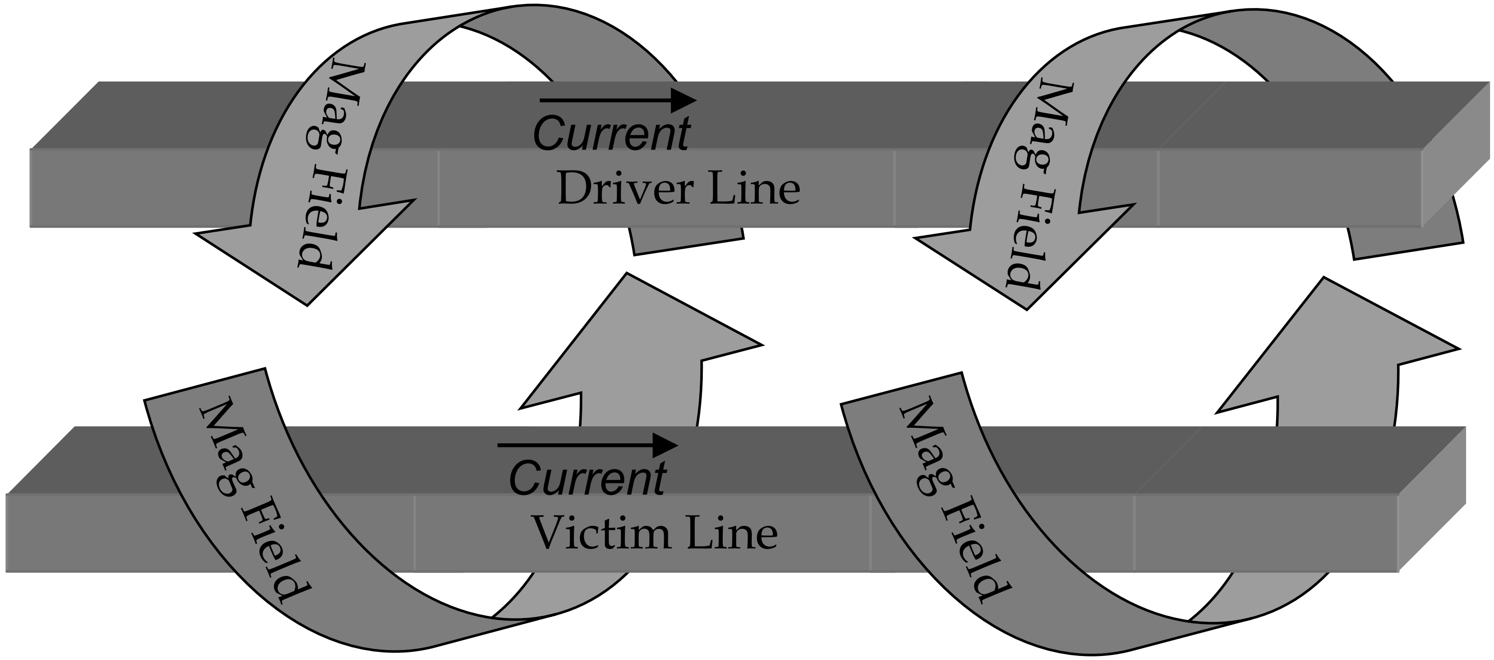
- Deterministic Jitter (DJ)

"Jitter with non-Gaussian probability density function. Deterministic jitter is always bounded in amplitude and has specific causes. Four kinds of deterministic jitter are identified: duty cycle distortion, data dependent, sinusoidal, and uncorrelated (to the data) bounded. DJ is characterized by its bounded, peak-to-peak value."

T11.2 / Project 1230/ Rev 10 Fibre Channel - Methodologies for Jitter Specification page 8.

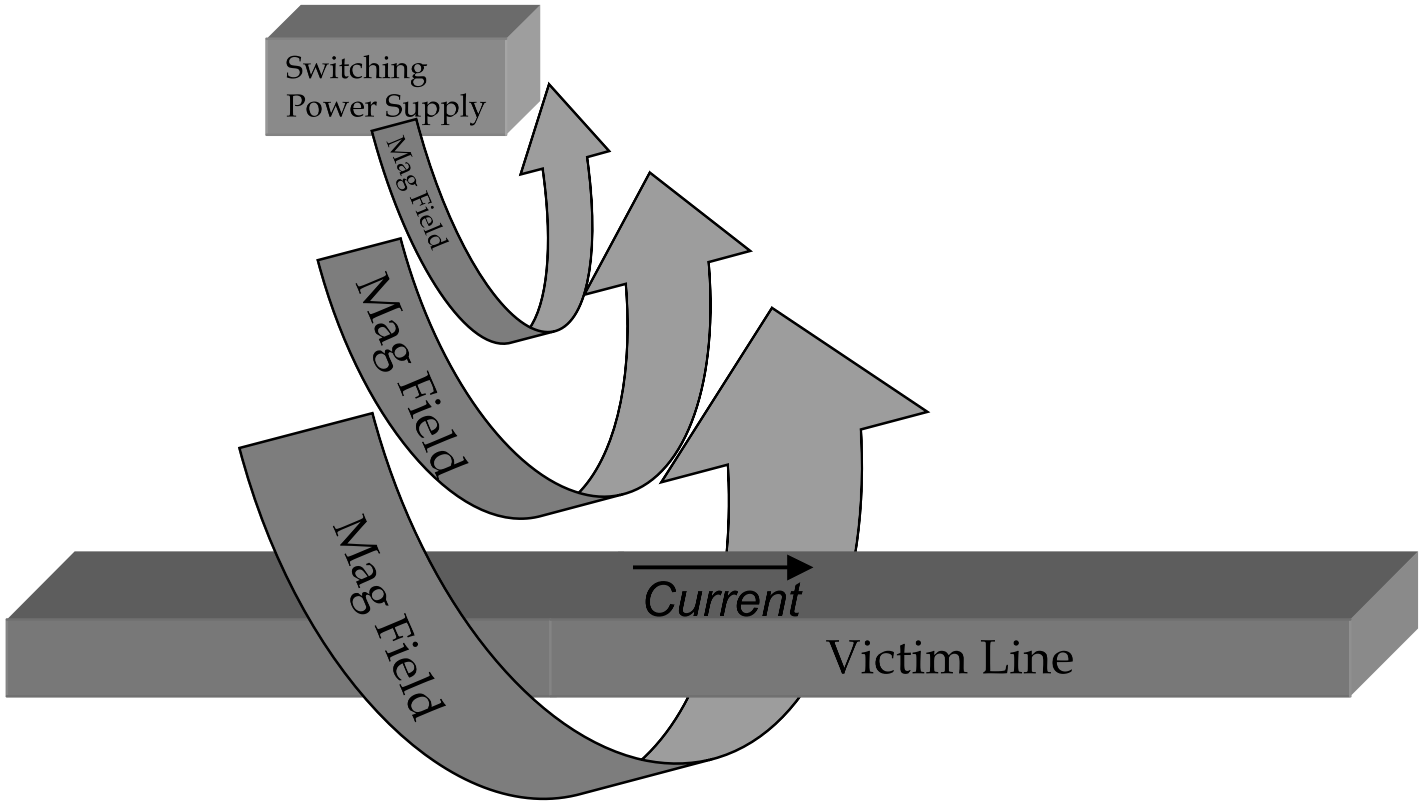


Where does DJ Come From?



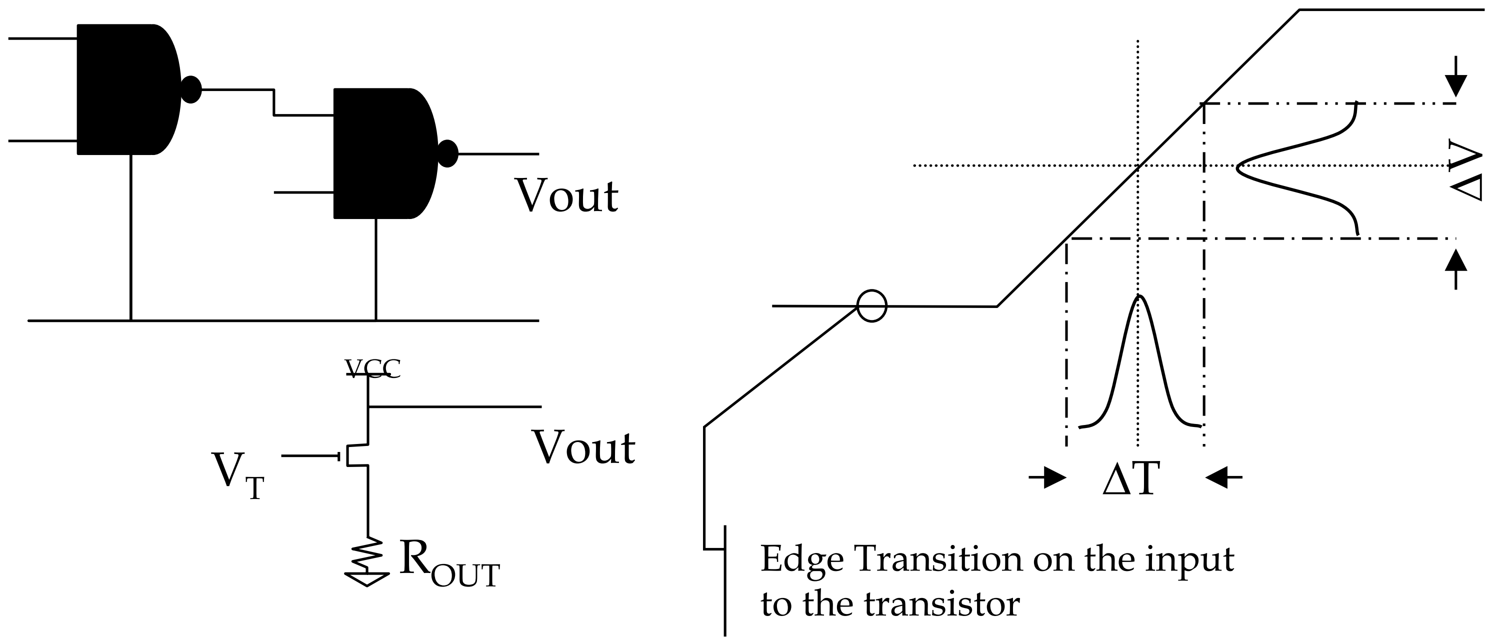
- Periodic Jitter from Cross talk
  - Victim line is affected by magnetic field from Driver line.
  - Incremental inductance of victim conductor converts induced magnetic field into induced current.
  - Induced Current adds (positively or negatively) to Victim Line current increasing or decreasing potential and thus causing jitter on Victim Line

Where does DJ Come From?



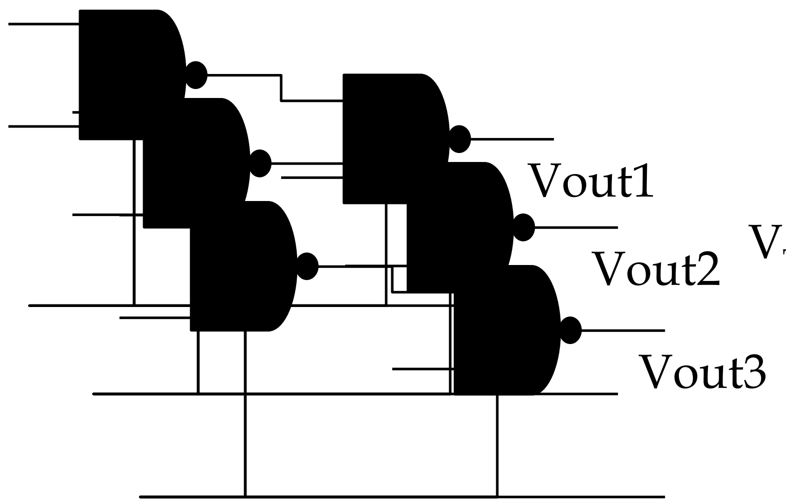
- EMI Radiation
  - Victim line is affected by magnetic field from EMI Source. This could be a power supply, AC Power line, RF signal source, etc.
  - As in cross talk induced jitter, the magnetic field induces a current that is added (positively and negatively) to the victim line current thereby effecting the timing of the signal on the victim line.

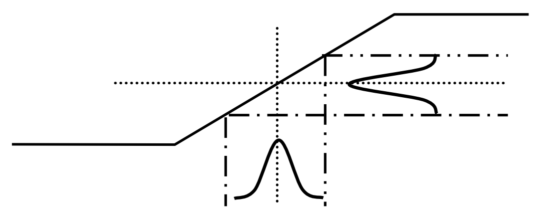
Where does DJ Come From?

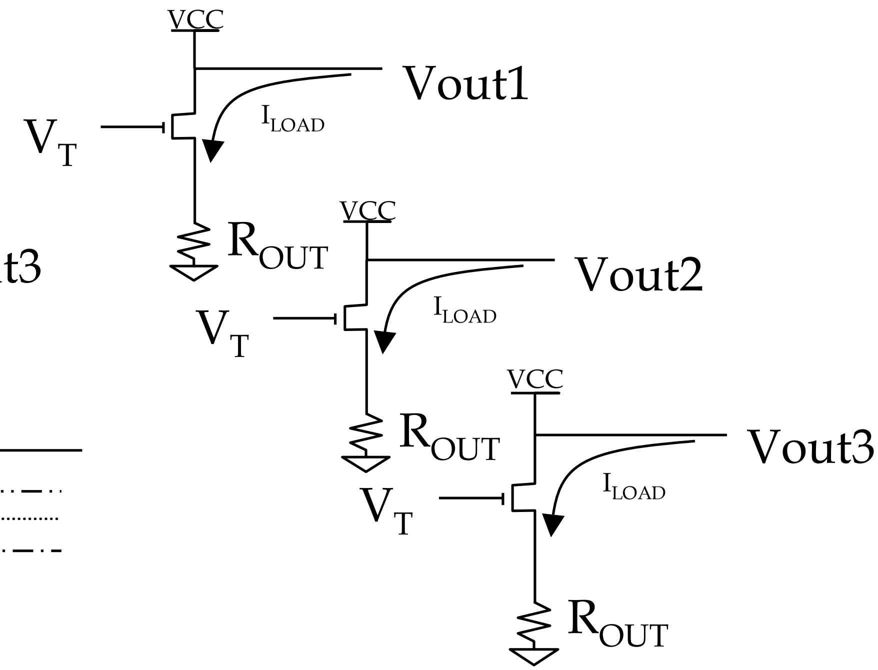


- Noisy reference plane
  - Noise in power planes can result in reference shifts in threshold voltages for downstream logic gates.
  - Resultant timing shift is proportional to slew rate of input signal.
  - The output transistor will switch when V_T is exceeded at the gate.
    - A change in ground reference at V_T will result in a shift in the required voltage to switch the gate thereby delaying or advancing the switch
  - VCO in PLL is sensitive to GND level variance.

Where does DJ Come From?







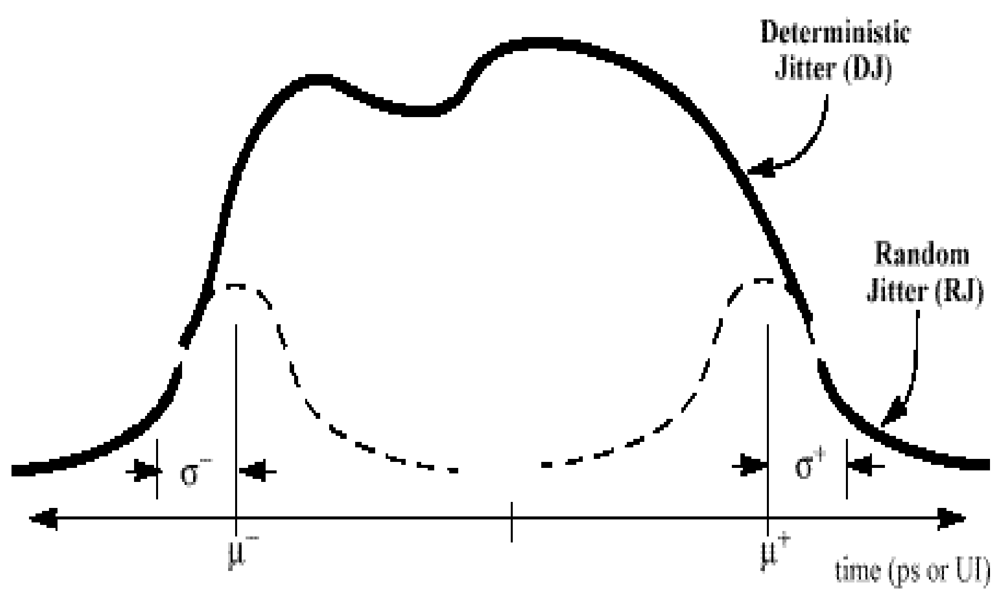
- Simultaneous Switching Outputs
  - If all output pins switch to same state, spike currents will be induced on VCC and on GND.
  - Spike Currents on Reference Plane can cause Threshold Voltage sense point to shift
  - Due to the pattern sensitivity and the bounded max. amplitude of edge jitter due to SSO, this is considered deterministic jitter.

What else is Jitter Composed of?

- Random (Gaussian) Jitter (RJ) –

"Jitter that is characterized by a Gaussian distribution…Random jitter is unbounded."

T11.2 / Project 1230/ Rev 10 Fibre Channel - Methodologies for Jitter Specification page 8

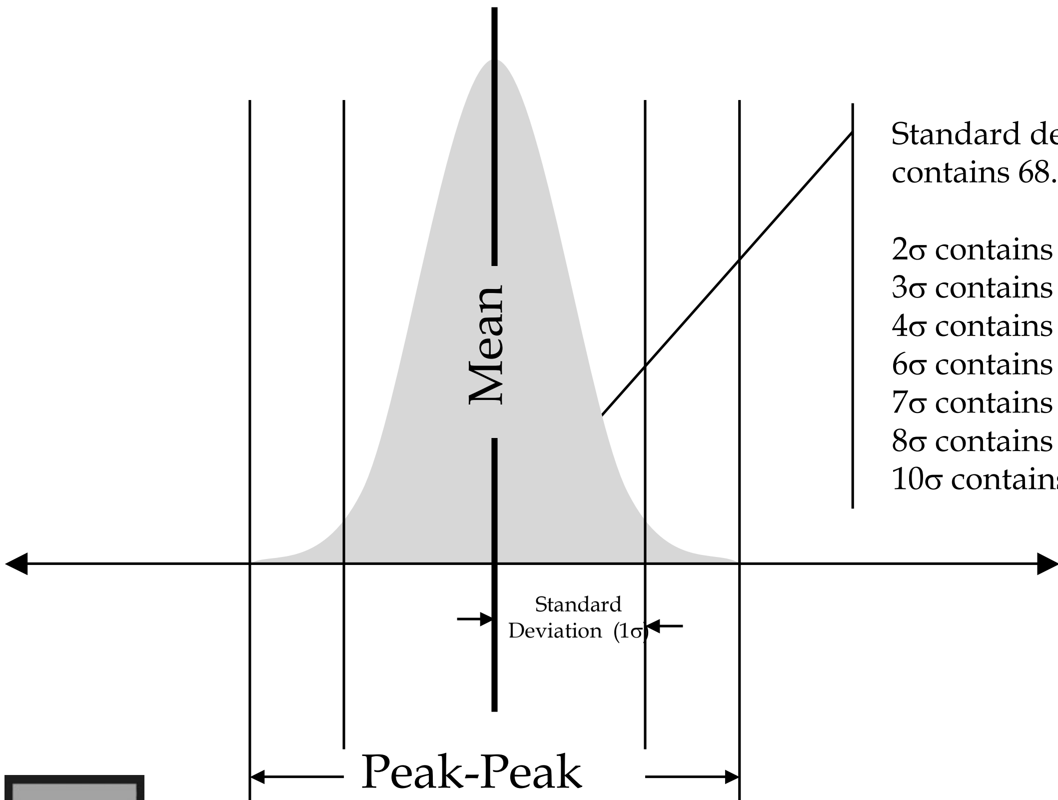


What else is Jitter Composed of?

- Where does Random Jitter Come from?
  - Random interferences in interface
  - Thermal vibrations of semiconductor crystal structure causes mobility to vary depending instantaneous temperature of material
  - Material boundaries have less than perfect valence electron mapping.
    - Imperfections due to semi-regular doping density through semiconductor substrate, well and transistor elements,
    - Imperfections due to process anomalies
  - Thermal effects of conductor material. Thermal vibration of conductor atoms effect electron mobility
  - Optical interference in interconnects.
  - And many more minor contributors such as:
    - cosmic radiation, etc...

Review of Basic Statistical Mathematics

- Intro to Gaussian Distributions
  - Before we can talk about measuring Jitter, it is important to understand Gaussian Distributions as it relates to probability.

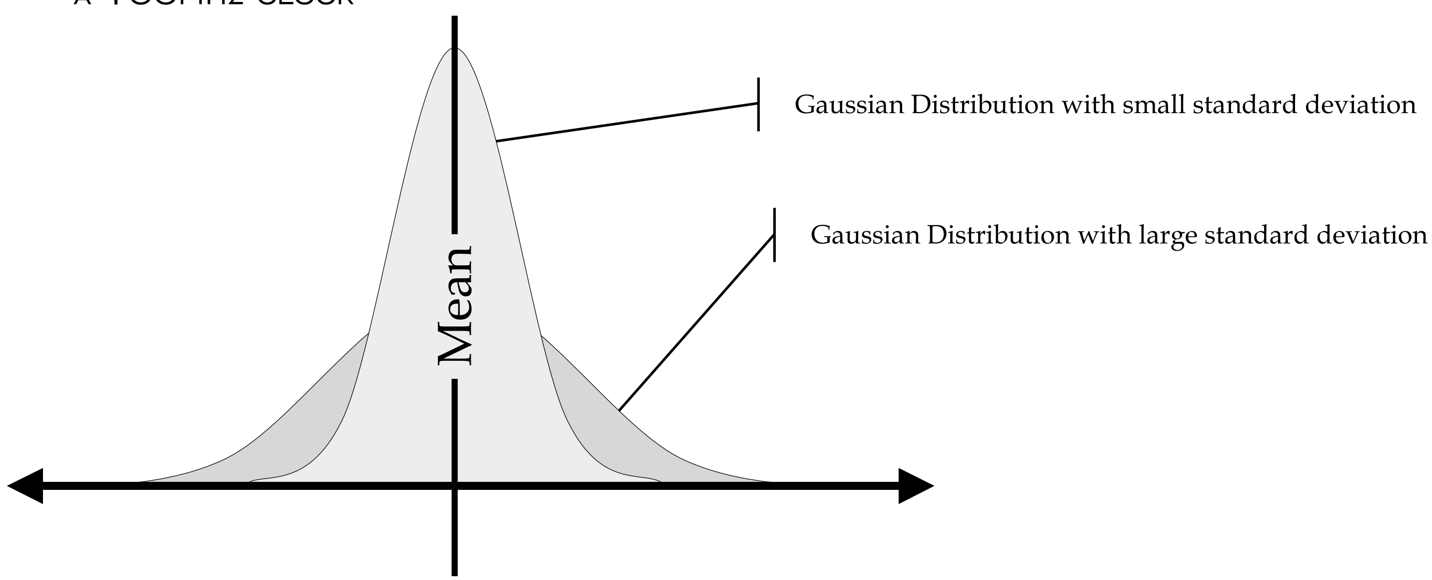


Standard deviation (1σ) is defined as the window in which contains 68.26% of all [measurements] to one side of the mean.

2σ contains 95.4% & of all measurements...
3σ contains 99.73% of all measurements...
4σ contains 99.99366% of all measurements...
6σ contains $(100-1.973\text{x}10^{-7})$% of all measurements...
7σ contains $(100-1\text{x}10^{-12})$% of all measurements...
8σ contains $(100-1.244\text{x}10^{-13})$% of all measurements...
10σ contains $(100-1.524\text{x}10^{-21})$% of all measurements...

More Gaussian Statistics

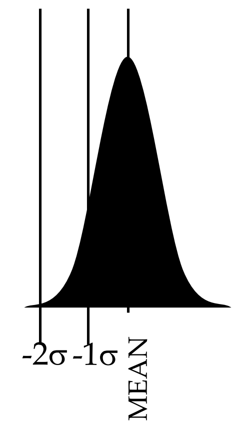
- Gaussian Statistics
  - It is important to note that in pure Gaussian mathematics, all possible measurements are assumed to be possible. However, for all practical purposes, the Gaussian model holds true in electronics for measurement populations not exceeding 10^{21}. This is equivalent to 20σ (single sided).
    - So, go ahead and use these Gaussian assumptions up to a reliability of about 20σ. After that, all bets are off as to the predictability of the measurement. 20σ reliability implies compliant operation for at least 321,502.06 years for a 100MHz clock



Why Standard Deviation?

- Standard Deviation is used to predict the occurrence of outlying measurements from the mean.
  - In electronics, it is important to know the frequency of occurrence of edges that are too early.
    - For example: 1GHz clock with $1\sigma = 10ps$
      - A clock period of 940ps occurs at least once every 507,614,213 cycles or about every 508ms
    - For example: 1GHz clock with $1\sigma = 50ps$
      - A clock period of 700ps occurs at least once every 507,614,213 cycles or about every 508ms

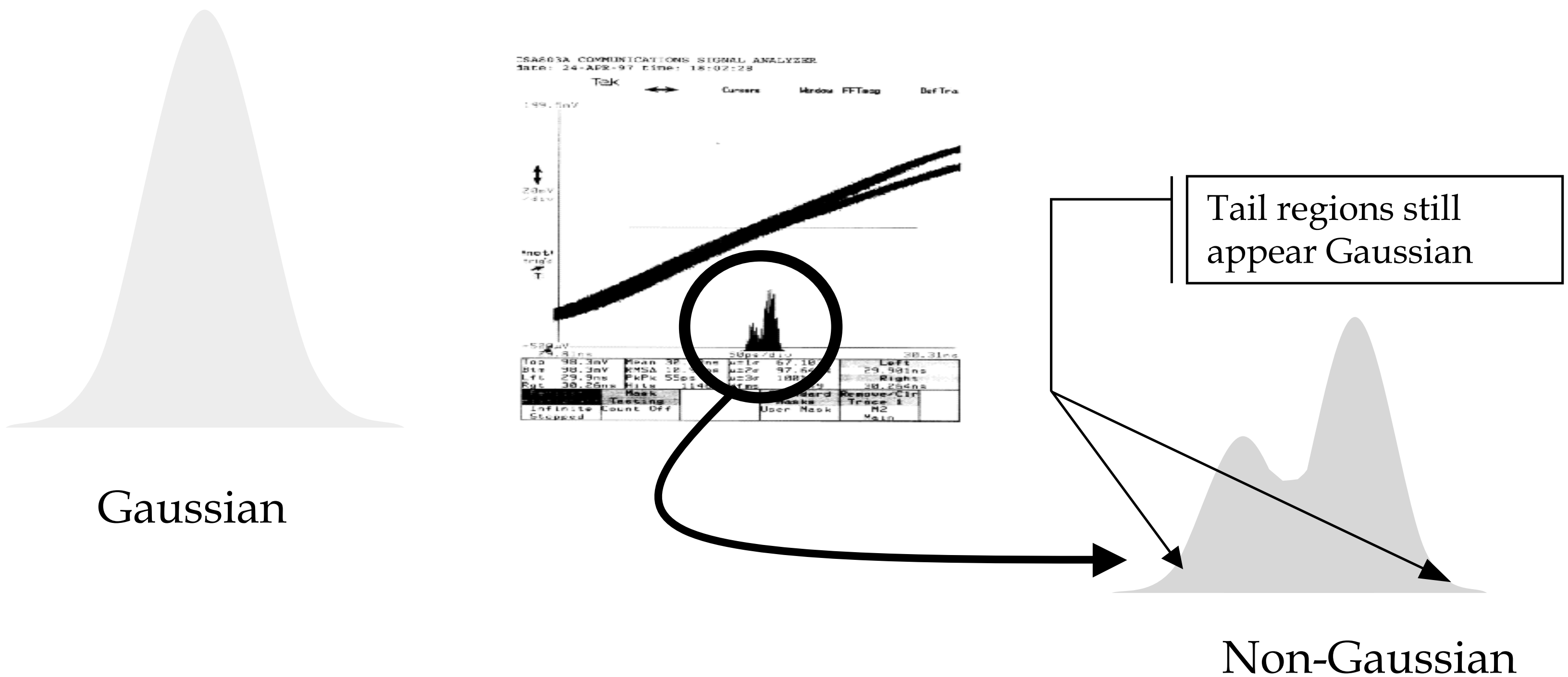
A measurement 2σ away from the mean will have a 4.6% chance of occurring. Thus, once every 15873 periods, the period is less than (mean - $2*1\sigma$). If we use the numbers from the previous slide, once every 250 periods the period is less than 9.97ns.



- The Catch…
  - This use of Standard Deviation (1σ) is only valid in pure Gaussian distributions. If any deterministic components exist in the distribution, the use of 1σ for the estimation of probability of occurrence is invalid.

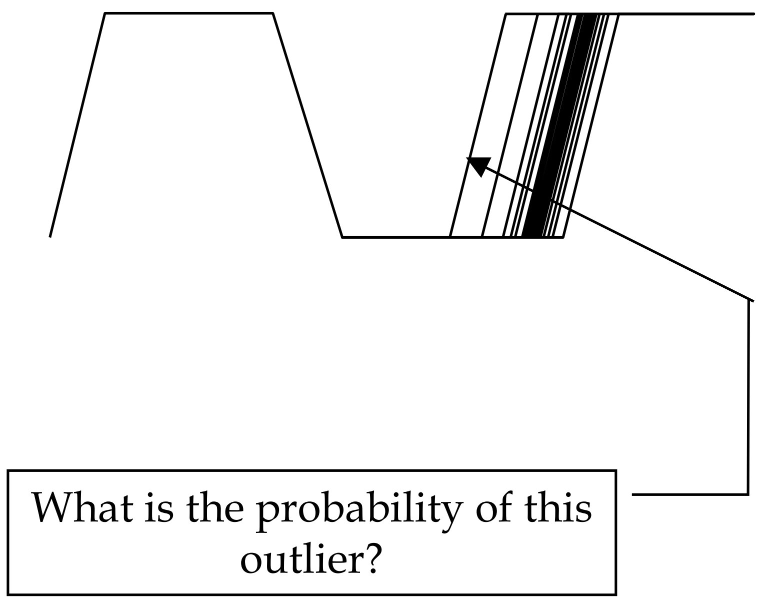
"Real World" Distributions

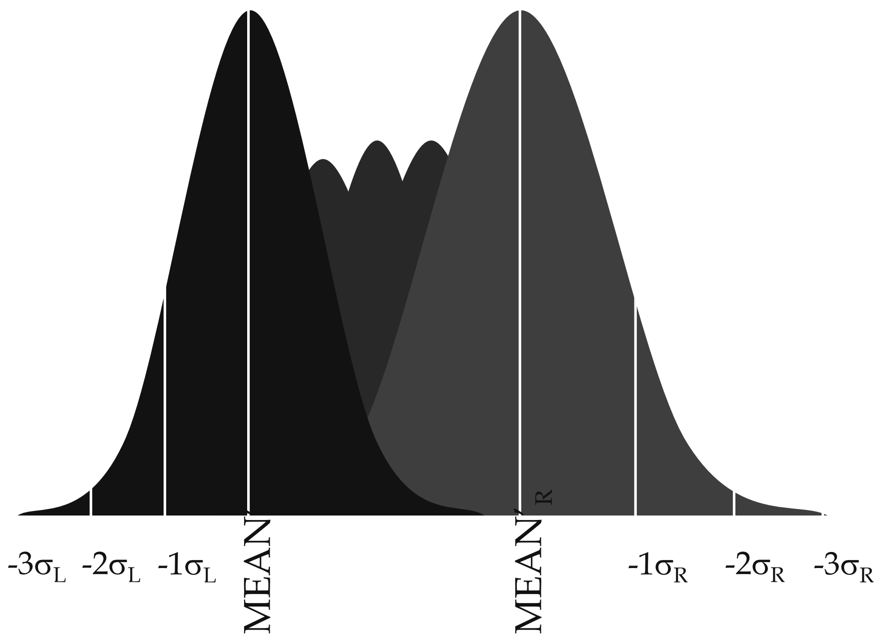
- In most cases, time measurement distributions are not entirely Gaussian.
  - Typically, some Deterministic/Systematic offset occurs to "mess-up" the distribution to make it Non-Gaussian



In non-Gaussian distributions, Gaussian assumptions apply to the tails (left most and right most regions) if and only if the equivalent 1σ of these tail region can be calculated.

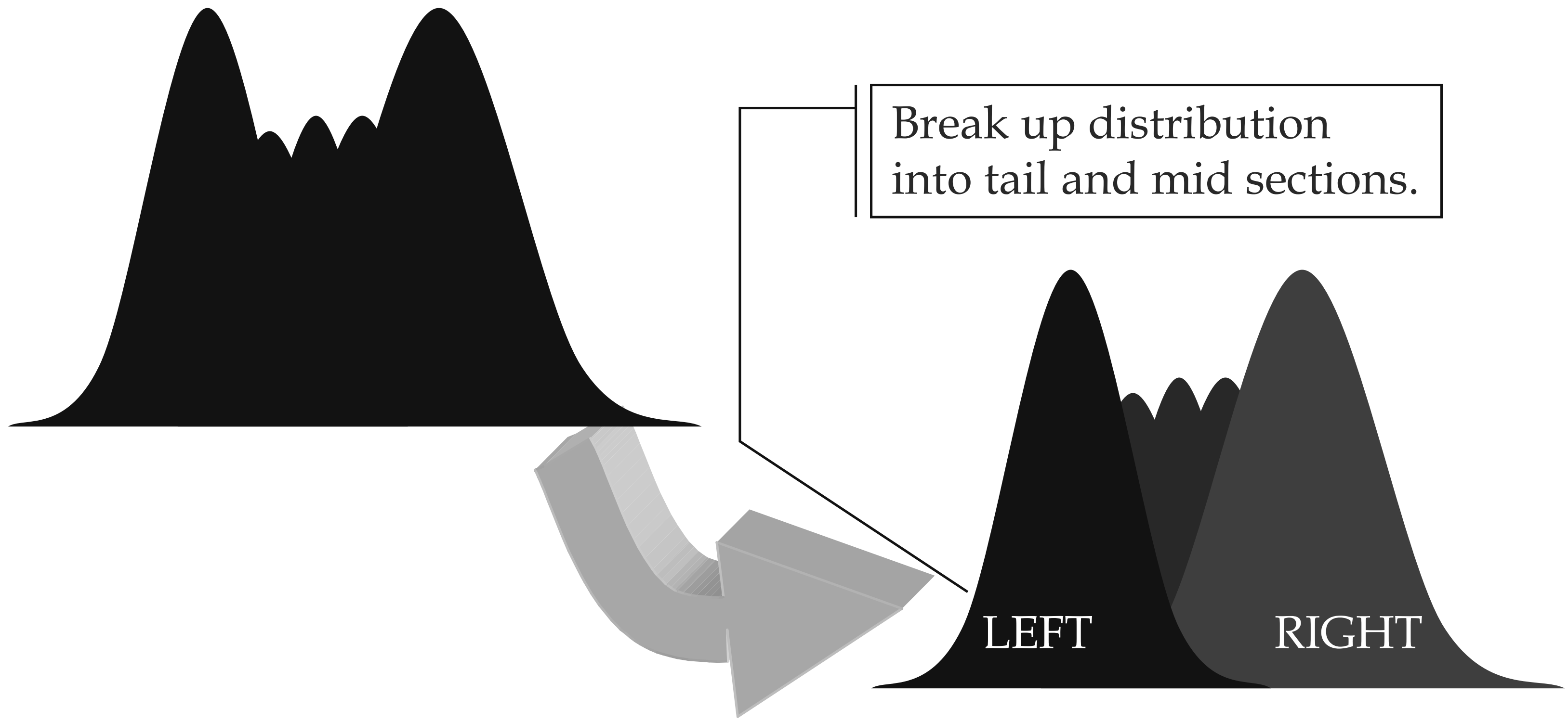
Using Jitter to Predict Outliers





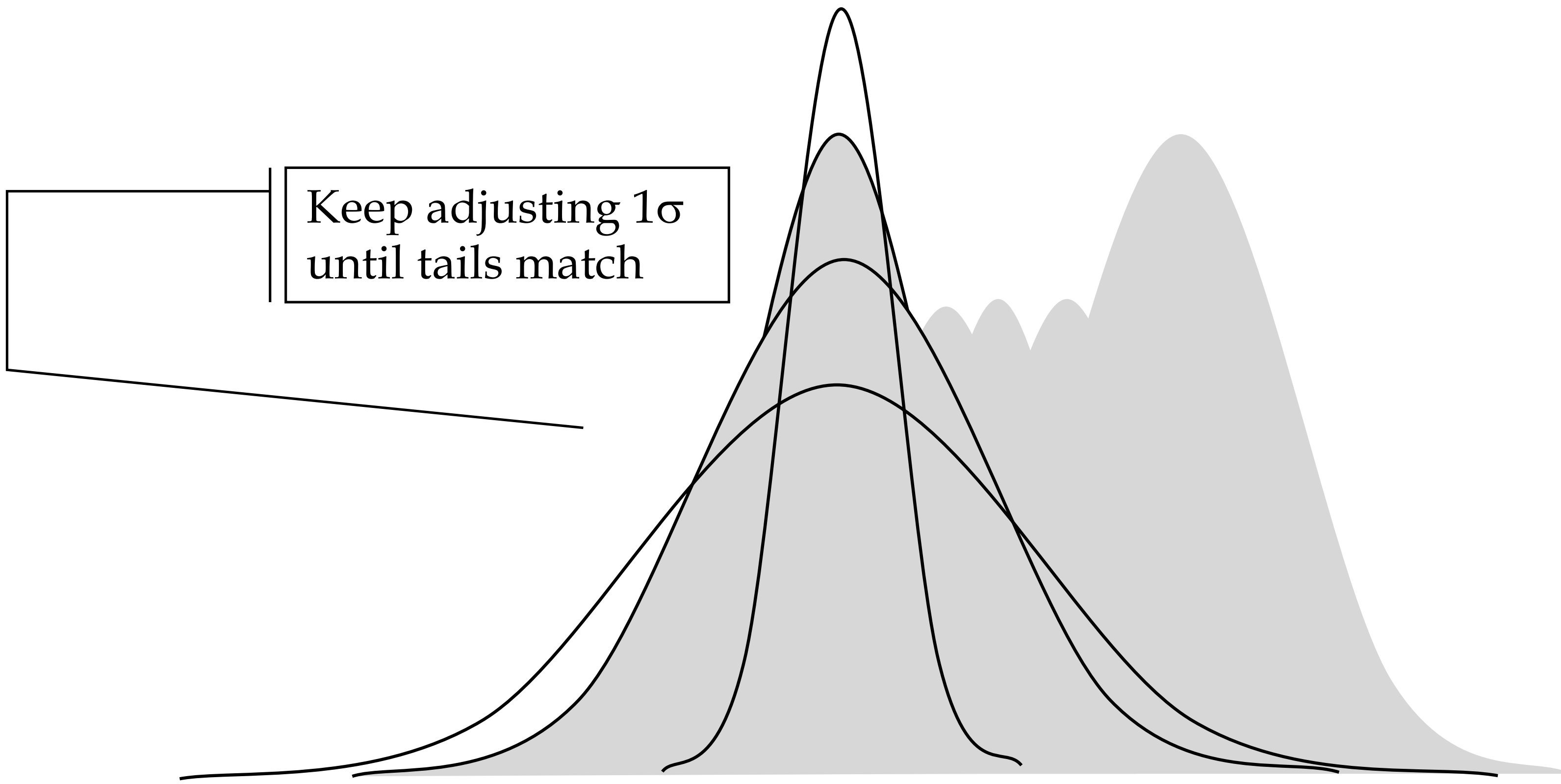
- In order to determine the probability of a measurement occurring at the $-3\sigma_L$ point, it is critical to determine the standard deviation that would correspond to a Gaussian Distribution with a identical tail region to that of our multimodal non Gaussian distribution.
  - Note that the matched Gaussians are not necessarily the same. Either tail can exhibit a larger standard deviation

Non-Gaussian Distributions



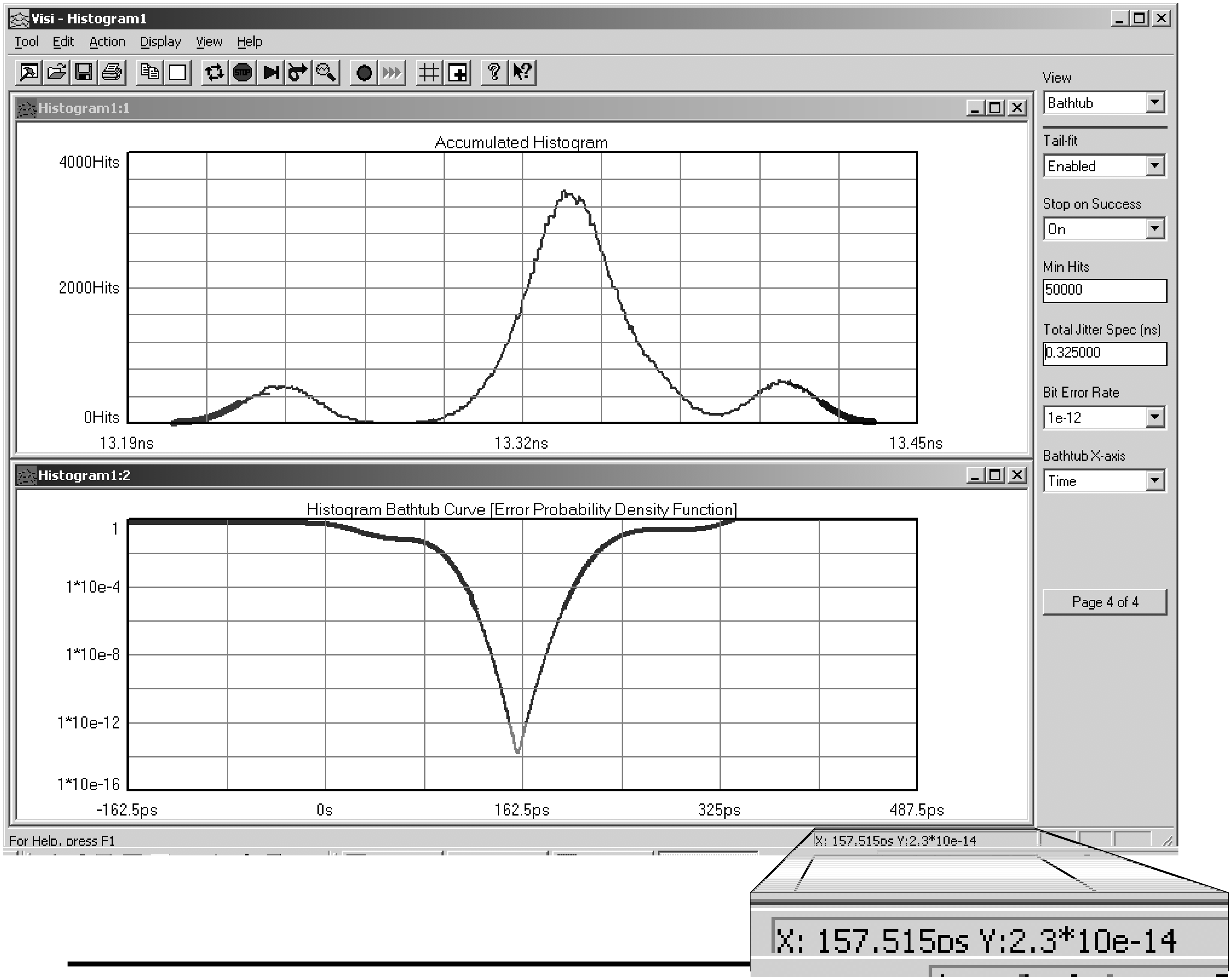
- Analyze distribution by looking at tail sections separately.
  - Allows for probabilistic estimations of out lying measurements
  - knowledge of Gaussian component (Random Jitter) on left side of multimodal distribution enables the calculation of the probability of short cycle measurements.
    - NOTE: Multimodal distributions are those distributions with more than one "hump". The non-Gaussian example shown here is referred to as bimodal. Some interesting information can be inferred from the shape of this distribution. Symmetric peaks imply equal probability of either mean point (left or right).

Determining Representative Gaussian Distributions

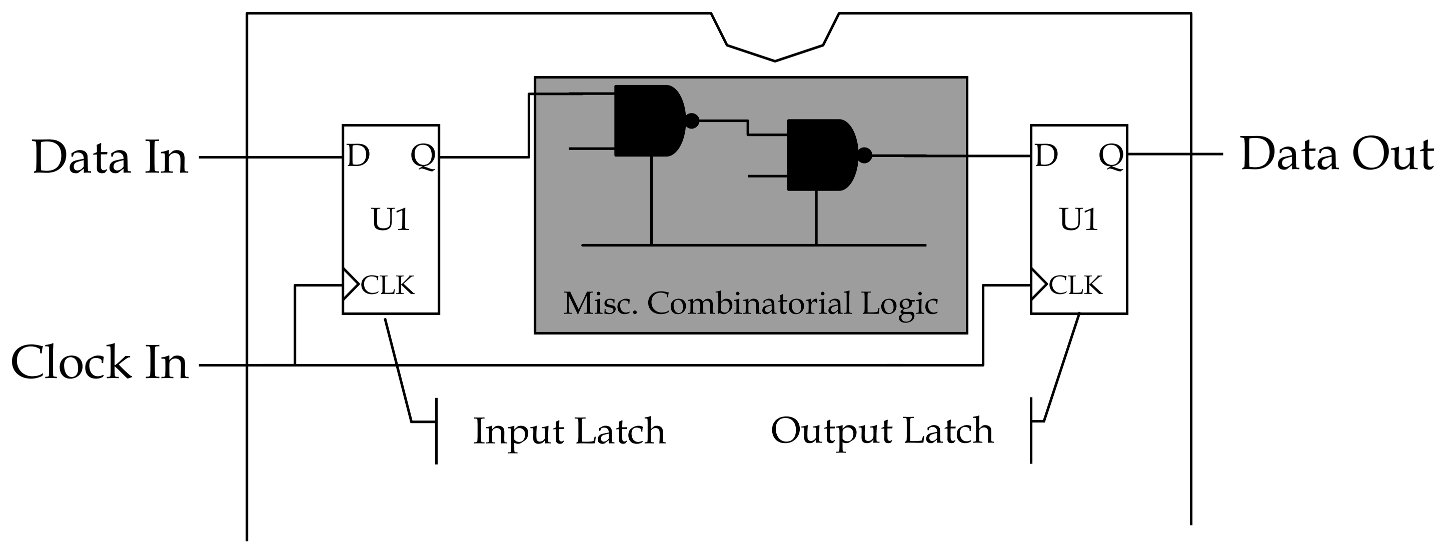


- TailFit™ algorithm enables the user to identify a Gaussian curve with a symmetrical tail region to that of the non-Gaussian distribution under evaluation.
  – Various curves are fitted against the distribution until an optimal match is found. Then, the 1σ of the matched curve is used as the standard deviation multiplier for that particular tail. This is repeated for both sides of the distribution.

An Example of Tail Fit Technique

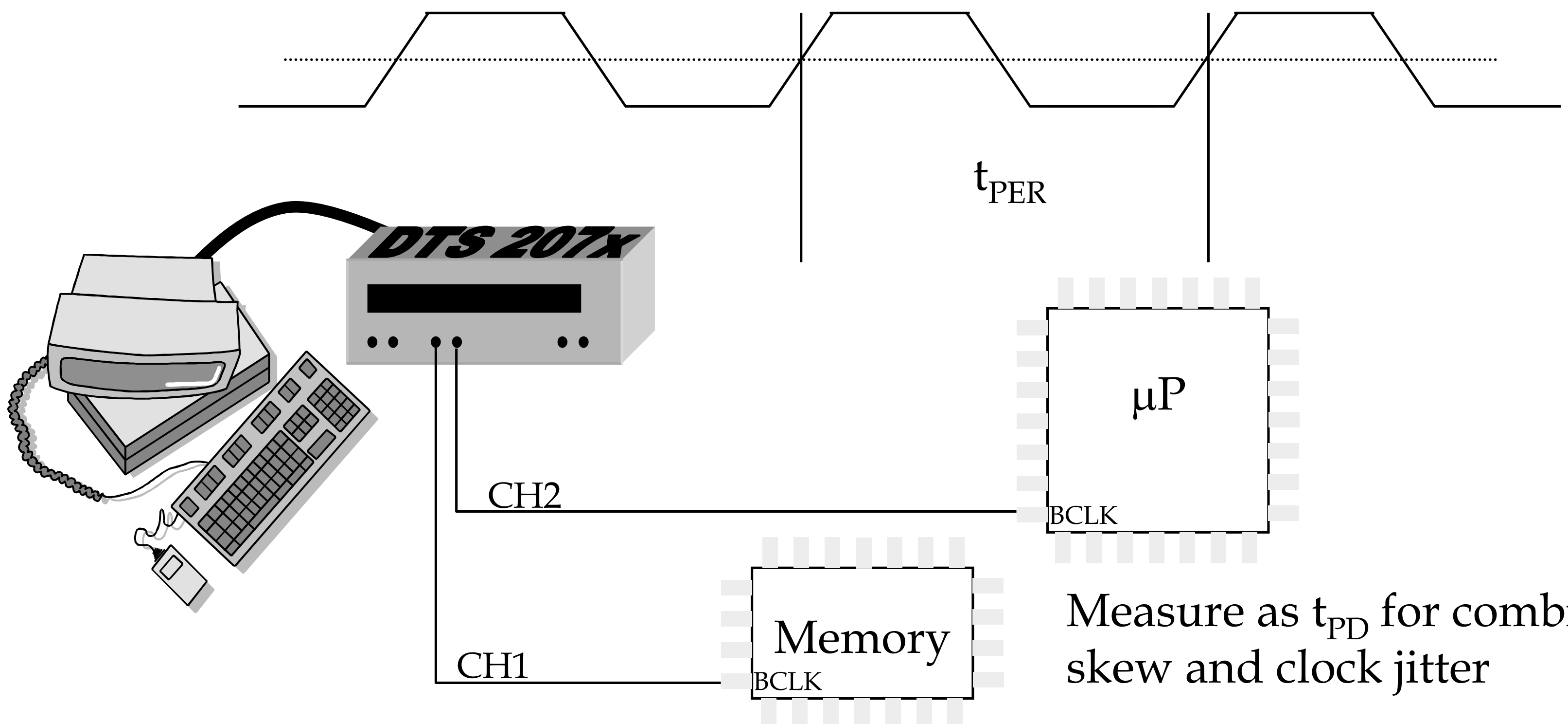


How does Clock Jitter Affect Systems?



- Typical Synchronous Device is susceptible to short cycle errors.
  - This device would latch the wrong data into the output latch if the period was to short. Therefore, the critical measurement for this device is period jitter (rising edge to next adjacent rising edge).
  - This is a typical problem for most synchronous devices and systems.
  - This is some times referred to as "Cycle to Cycle"
    - See Appendix for Intel ® Pentium II & III spec and Tektronix application notes for further details

Period Stability (Period Jitter)



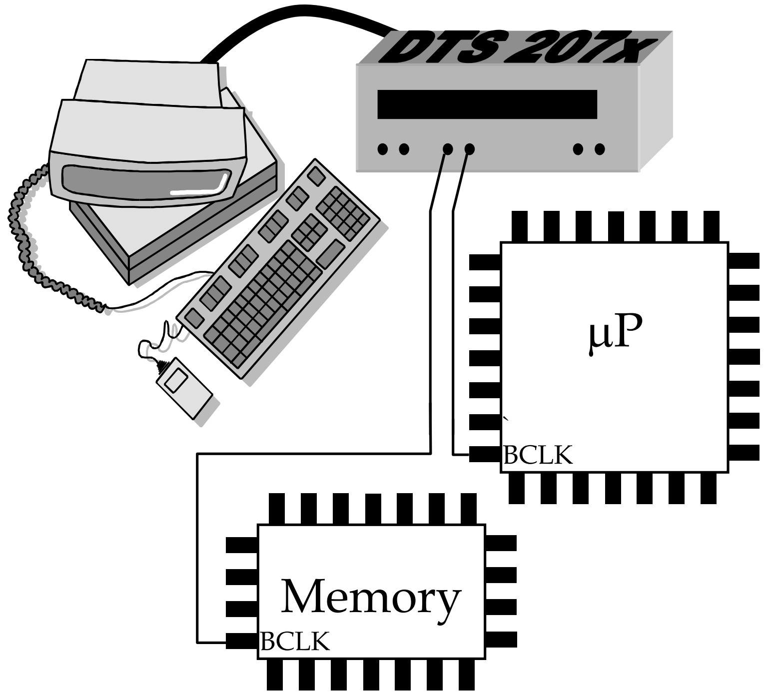
Measure as t_{PD} for combined skew and clock jitter

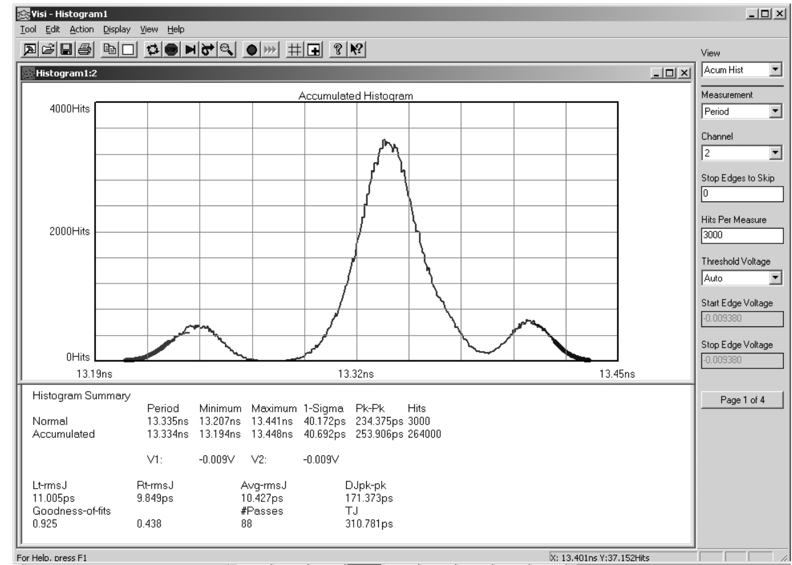
- Intel Period Stability Specification:

  "...should be measured on the rising edges of adjacent BLCKs crossing 1.25V at the processor core pin. The jitter present must be accounted for as a component of BCLK timing skew between devices."

  Intel® Pentium® II Datasheet, pg 27

Example Debug Session



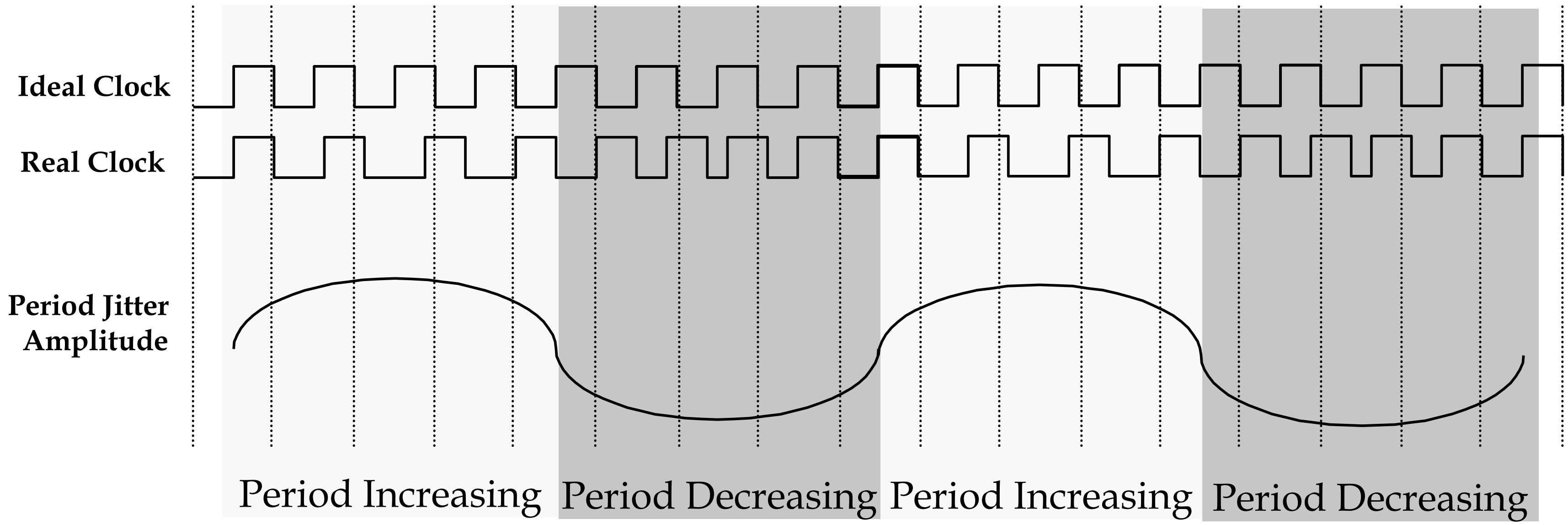


- In this example, note the presence of DJ.
  - The next step would be to determine if the DJ is due to cross talk, pattern dependency, or EMI interference.
  - Use Accumulated Time Analysis to determine Frequency of PJ
  - If PJ is a multiple frequency of clock, use a pattern marker to measure periods relative to the pattern running on the device/system to determine where, if at all, in the pattern the jitter is a maximum.

What is Accumulated Time Analysis™?

- The key to Periodic Jitter Detection.
  - Periodic Jitter is deterministic jitter that is typically caused by an EMI interference or cross talk.
  - Periodic Jitter has both Frequency and amplitude.
    - Amplitude can be expressed in both single period deviation or cumulative deviation.
  - Accumulated Time Analysis is a technique that uses accumulated jitter to determine the presence of periodic jitter.
  - Using ATA, the user can quickly and simply measure the cumulative amplitude and frequency of modulation for all Periodic Jitter elements riding on the signal.
  - Using a patented normalization technique, the user can also see the worst case period deviation due to each of the PJ components.
- What is Cumulative Jitter?
  - Periodic Jitter has the effect of increasing the period and decreasing the period of a clock over time.

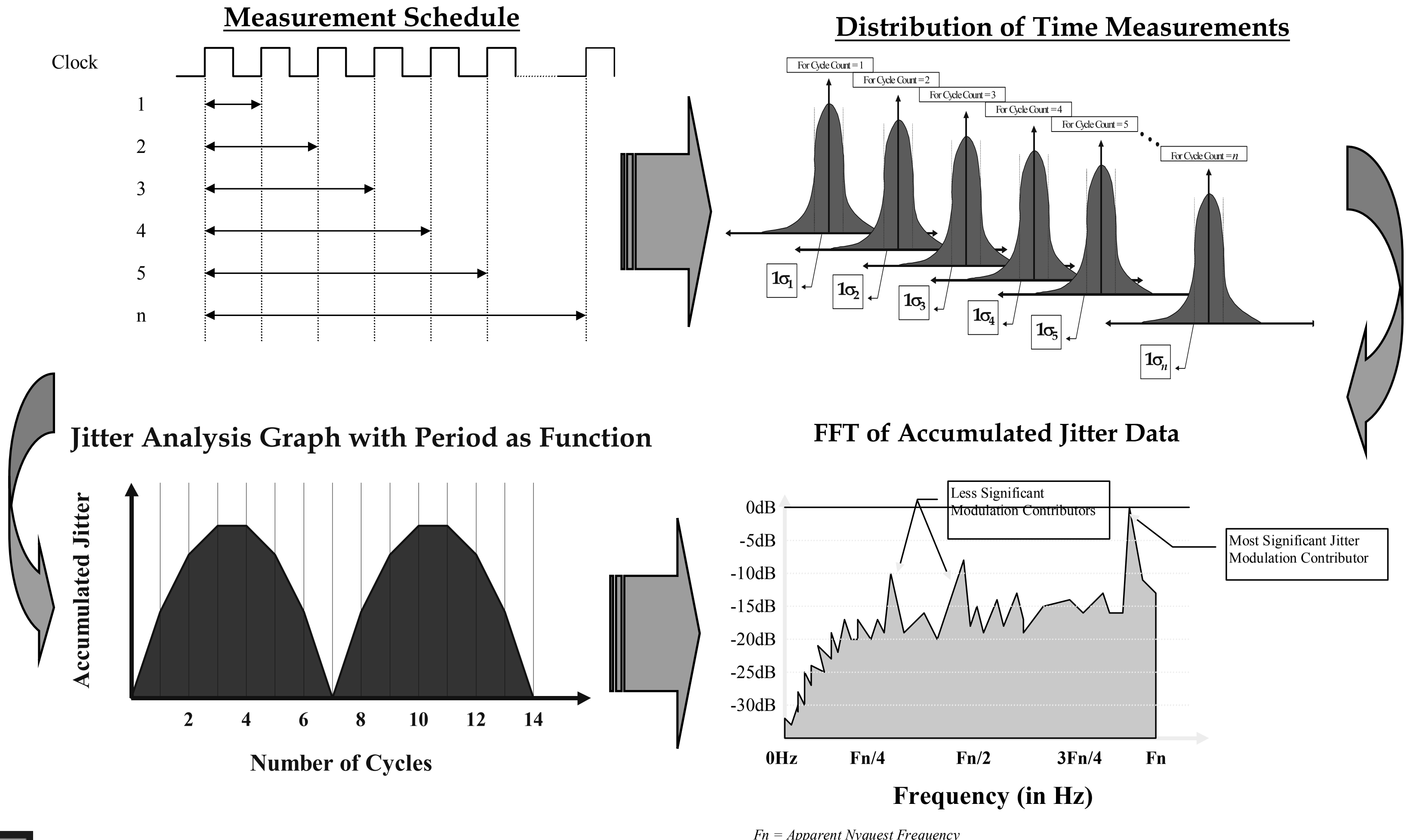
The effect of a Periodic



- Period Increasing
  - In this section the period of the modulated clock is increased from the ideal. Notice how much longer the elapsed time for 5 periods.
- Period Decreasing
  - In this section the period of the modulated clock decreases from the ideal. The net effect of the shorter periods results in a canceling out of the increased periods from the prior section. Note that the same number of clocks is completed after both sections.

It is important to note that the sampling of the waveform must be random so as not to filter any periodic elements.

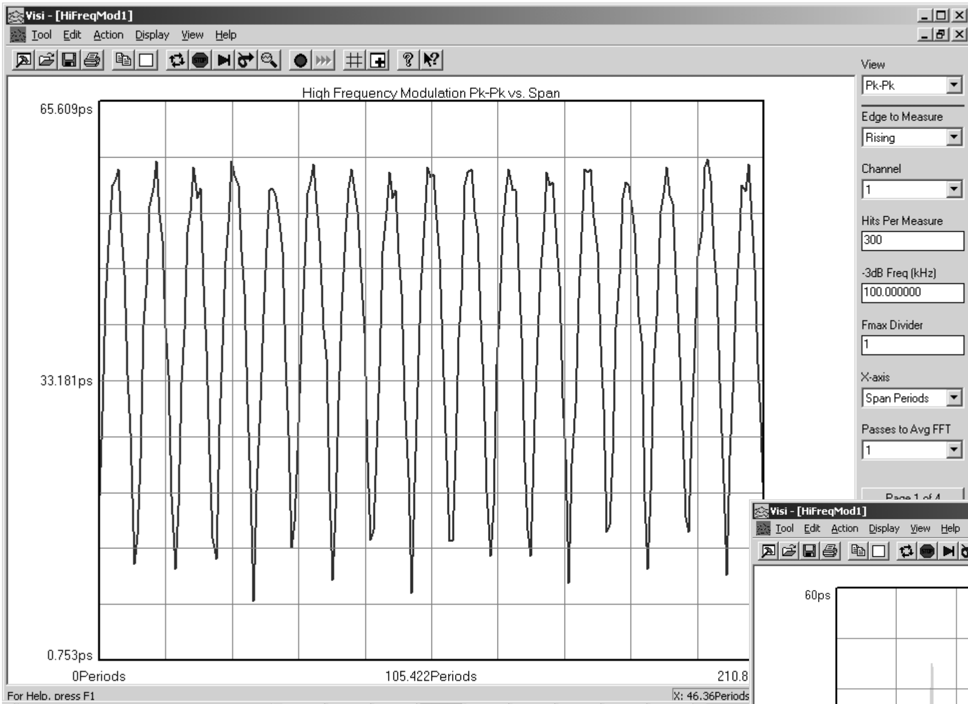
Accumulated Time Analysis™



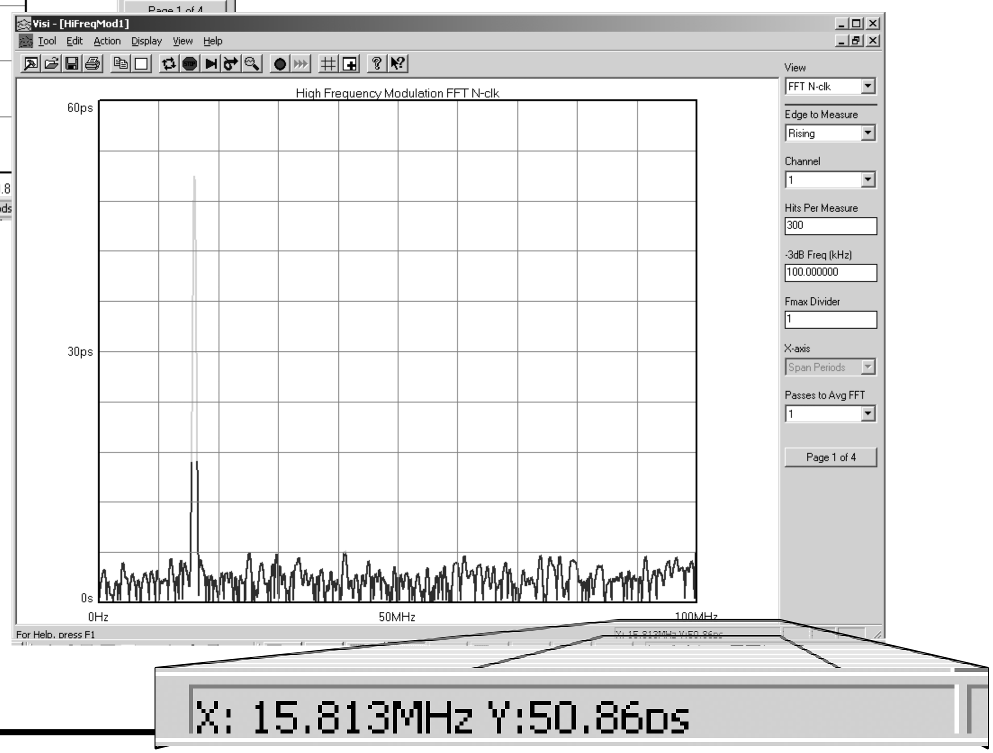
What is an FFT?

- Fast Fourier Transforms (FFT) are used to translate time domain data to Frequency domain data.
  - FFTs are used in oscilloscopes to genenerate a frequency domain plot of the waveform under test.
  - *See Section 4 of this manual for a complete discussion on our implementation of FFT.*
- Wavecrest's FFT of the modulation domain
  - The modulation domain is a plot of the accumulated jitter versus time.
  - The FFT of the modulation domain will show the frequency components of the modulation.
  - Spectral peaks in the FFT of the modulation domain identify Frequency Modulation (FM) components which are riding on the signal under test.
  - The data can be normalized such that the spectral peaks' amplitude will be proportional to it's effect on period jitter.

Using Accumulated Time Analysis



The modulation domain plot to the left indicates a strong periodic with a cumulative jitter amplitude of 50ps

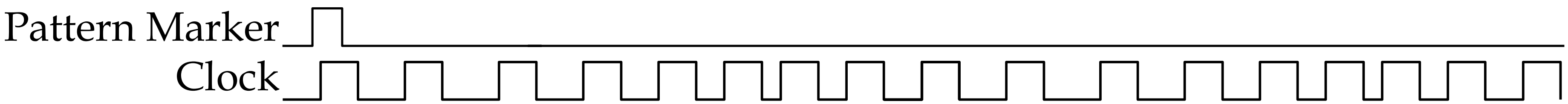


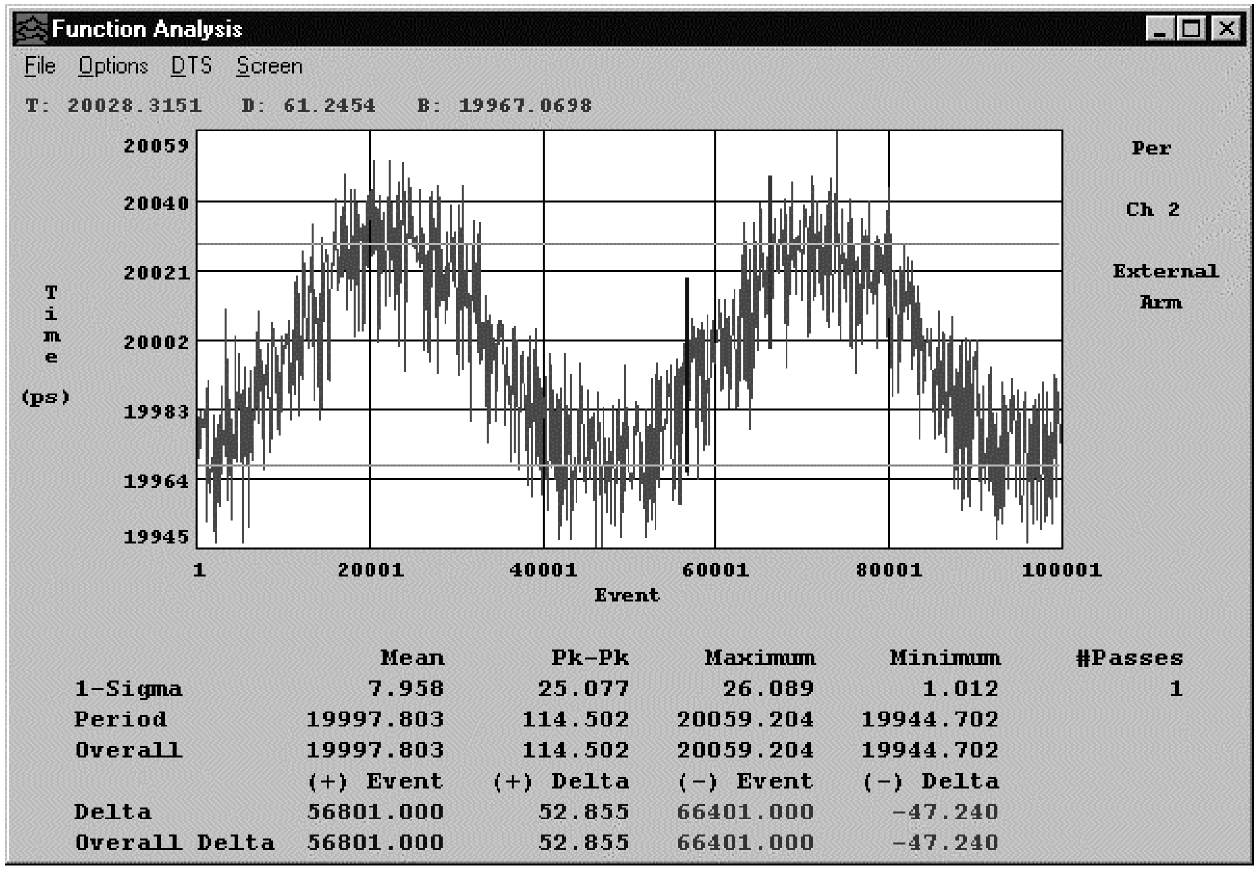
The frequency domain plot to the right indicates a strong periodic at about 15.8MHz. This tool can also be configured to normalize the peak amplitudes of each periodic element to it's exact effect on a single period. This is called 1-clock normalization.

Pattern Dependant Jitter

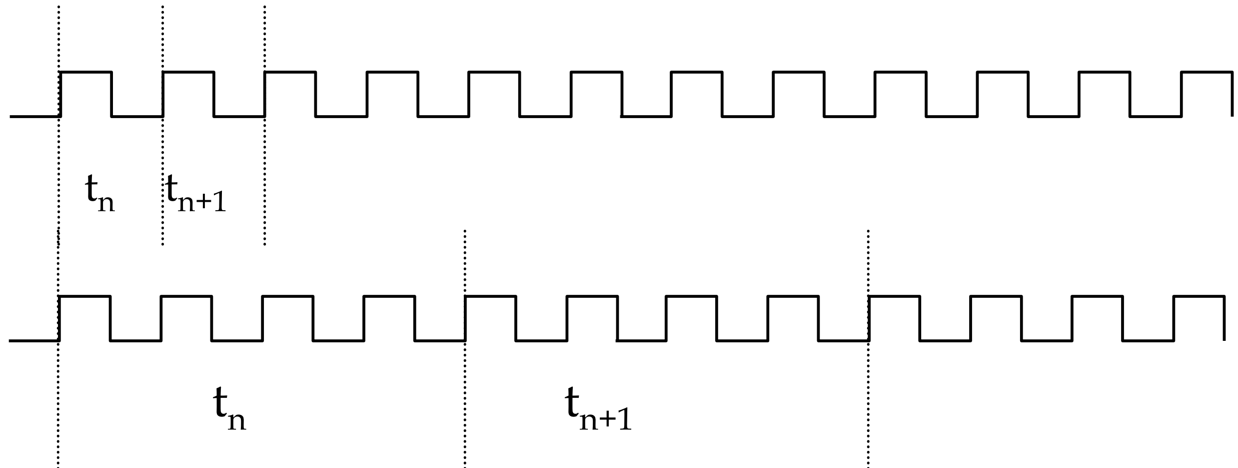
- In some cases, the jitter on the clock could be correlated to other electronic activity near by.
  - This could be the case in an imbedded PLL application in which some other circuit in the ASIC is causing the internal PLL to jitter tremendously.
  - In the case of a system design, perhaps another part of the circuit board is emitting an excessive amount of EMI that is interfering with the operation of the PLL or is inducing modulation on the traces distributing the clock signal.
- Debug this using Function Analysis
  - The user can also debug using an oscilloscope and a pattern marker.
    - For sampling oscilloscope, make sure the stability of the reference does not exceed the DJ being diagnosed
    - For real time sampling oscilloscope, make sure the record length completely captures one execution of the pattern.
  - Wavecrest Function Analysis Tool allows the user to look at each and every period after a pattern marker to evaluate pattern dependant jitter.

Using Function Analysis



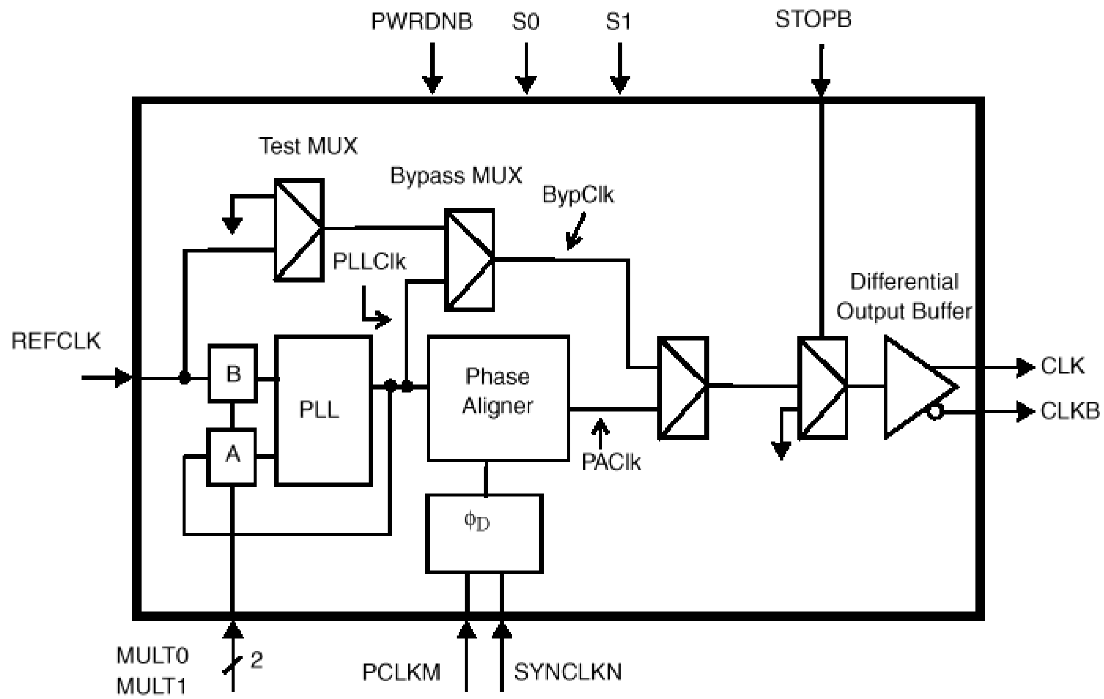


Adjacent Cycle Jitter (Rambus Jitter)



- Adjacent Cycle Jitter
  - Referred to by Rambus as "Cycle-to-Cycle"
    - Since this is inconsistent with established definitions from Tektronix, Intel, Hewlett Packard (Agilent),Wavecrest and many others, we will simply refer to this jitter phenomena as "Adjacent Cycle Jitter"
  - Adjacent Cycle Jitter is the worst case period deviation from one period to the next adjacent cycle. Measurement must be taken at exactly the same voltage for stop as well as start. Rambus requires that 10,000 adjacent periods be analyzed for compliance.

Why test Adjacent Cycle Jitter?

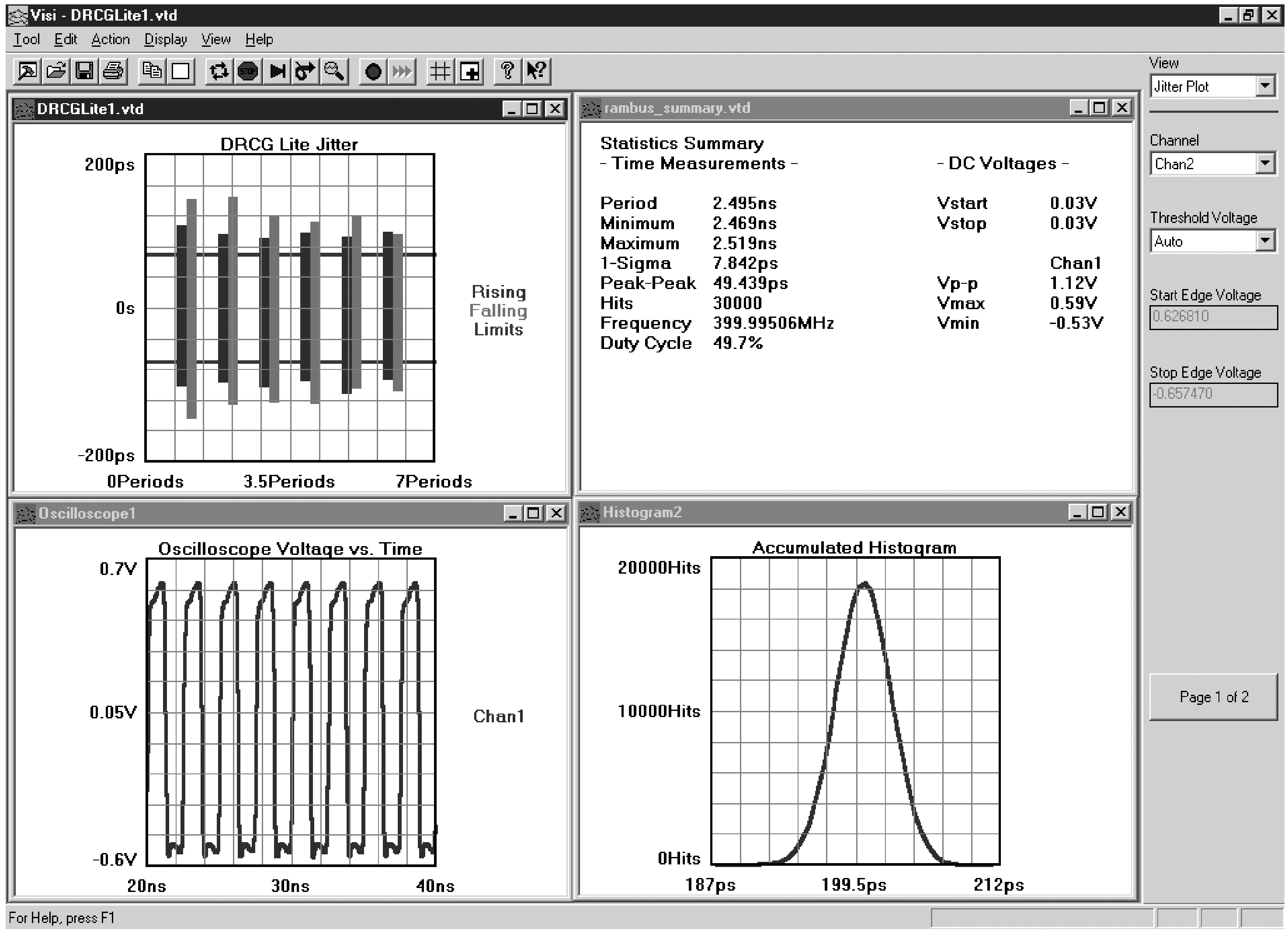


- Phase Aligner can adjust period based on instantaneous phase shift in Rambus® memory circuit relative to the rest of the system and/or system clock.
  – User can disable Phase Aligner to characterize PLL independently. Then, user can test Phase Alignment circuitry using DTS550 to force phase shift condition.

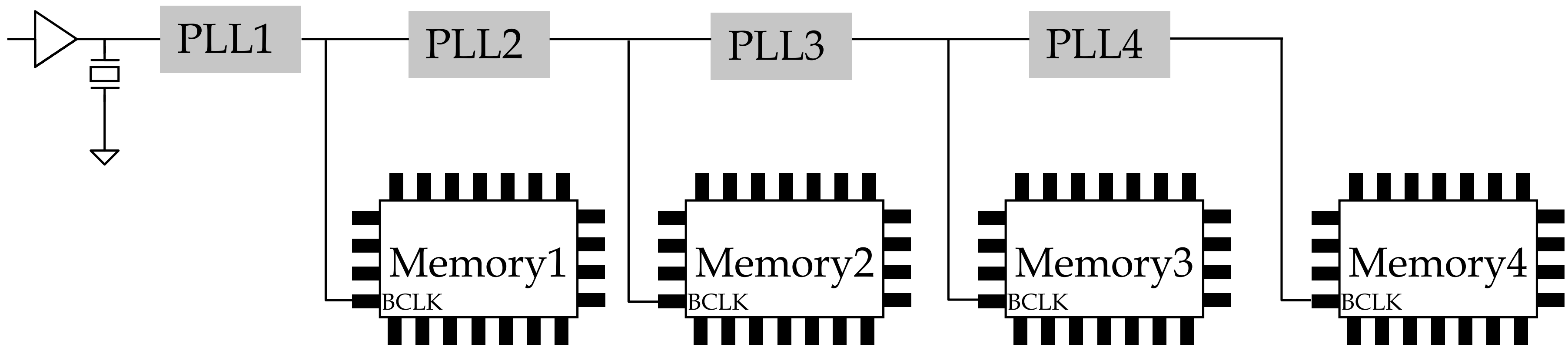
How do you measure Adjacent Cycle Jitter?

- Real Time Oscilloscope.
  - Jitter spec is 50 ps and rise time can be as fast as 160ps.
    - Therefore, for enough samples (3 per edge) on each rising/falling edges, use a real time oscilloscope with a sampling rate of at least 33ps. This is equivalent to a 33GHz Real Time Sampling Oscilloscope.
    - For the accuracy of 50ps, try to get a real time sampling oscilloscope with at least 10x the noise floor and 10x the resolution. So, the ideal real time oscilloscope should have a sampling rate of at least 200GHz.
    - Anything less is a coarse estimate.
- Wavecrest SIA3000
  - Measures Adjacent Cycle Jitter directly
    - Measure cumulative adjacent periods with counters for each measurement
    - Get better than 200fs of resolution and better than 1ps of accuracy
  - Perform full compliance in less than a second.
    - Test all frequencies and voltages
    - Export results, in tabular format, to Standard RAMBUS® Excel spreadsheet
  - See all orders of cumulative adjacent cycles (1-6) using Rambus DRCG tool.
  - Use advanced analysis routines to debug any jitter anomalies.
    - Separate jitter components to identify root cause.
    - Identify Periodic Jitter frequency (μHz to GHz) and amplitude (As to s)

RAMBUS® DRCG Tool



What Happens to Downstream Devices?

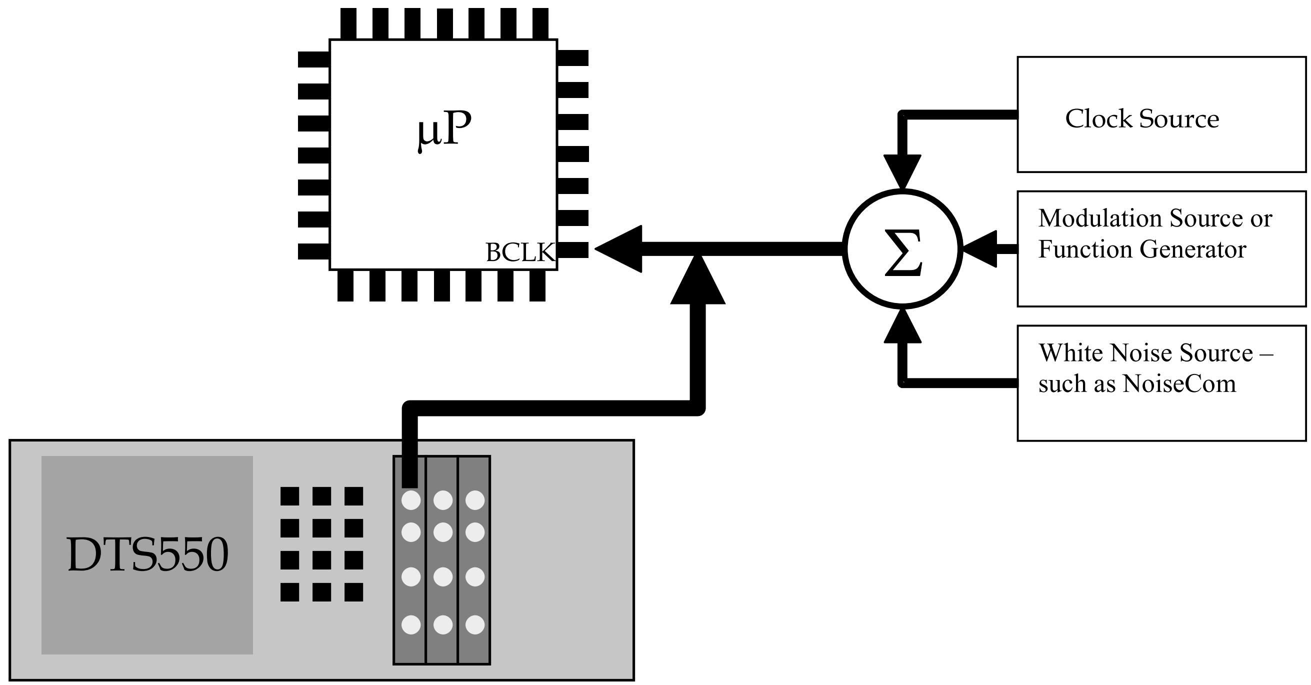


- PLL Bandwidth
  - All PLL devices have a cutoff frequency which defines the maximum modulation frequency that PLL can track. Modulation frequencies above the cutoff frequency are simply ignored.
    - So, if EMI radiation of 2MHz were induced after PLL1, and PLL2 has a cutoff frequency of 500kHz, then, Memory 1 will see the modulation on it's clock input while Memory 2 will not.

  (Watch for future Wavecrest tools to measure PLL Bandwidth, loop response, dampening coefficient and much, much more.)

- Jitter Tolerance
  - The downstream devices may be susceptible to many forms of jitter caused by the circuit design, ambient environment or even the PLL driving it. Jitter Tolerance is a measure of how much Jitter a device can handle and still function properly.

Jitter Tolerance In a Digital Network

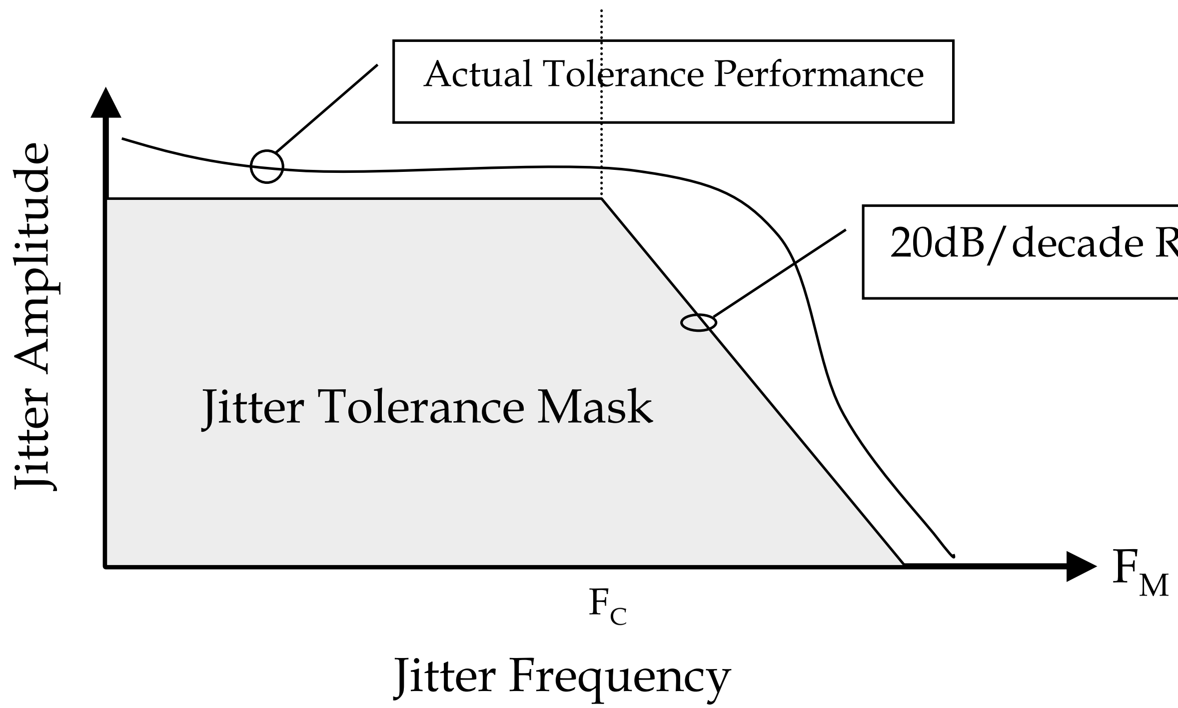


- Substitute Jitter Generator for PLL signal at each device to test maximum allowable jitter.
  - Can use a series of instruments including a clock source, modulation source and White Noise Source.
  - Can also use Wavecrest DTS550 Jitter Generator for up to 1 GHz clock emulation with full jitter programmability.

Jitter Tolerance Testing

- Sweep through frequency range for modulation sensitivity testing.
  - Many internal circuits feature an embedded PLL
  - Since all PLL devices have a bandwidth, it is important to sweep the modulation frequency through several different frequencies to determine specific sensitivities.
- Use several different Jitter combinations.
  - Increase psuedo random jitter to test for Random Jitter,
  - Sweep Periodic Jitter through several frequencies and amplitudes.
  - Check Power sensitivities to jitter tolerance.
  - Check thermal sensitivities to jitter tolerance.

Jitter Tolerance Map



- Input Jitter Tolerance vs. Frequency of Modulation
  - Sweeping through several frequencies to determine frequency sensitivities:
    - Determine cutoff Frequency (F_C). This is the frequency at which the PLL will begin to filter out the input modulation due to the PLL circuits natural loop feed back response.
    - Determine sensitivities within the entire system to specific frequency/amplitude sensitivities.

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Jitter Analysis of Data Communication Devices

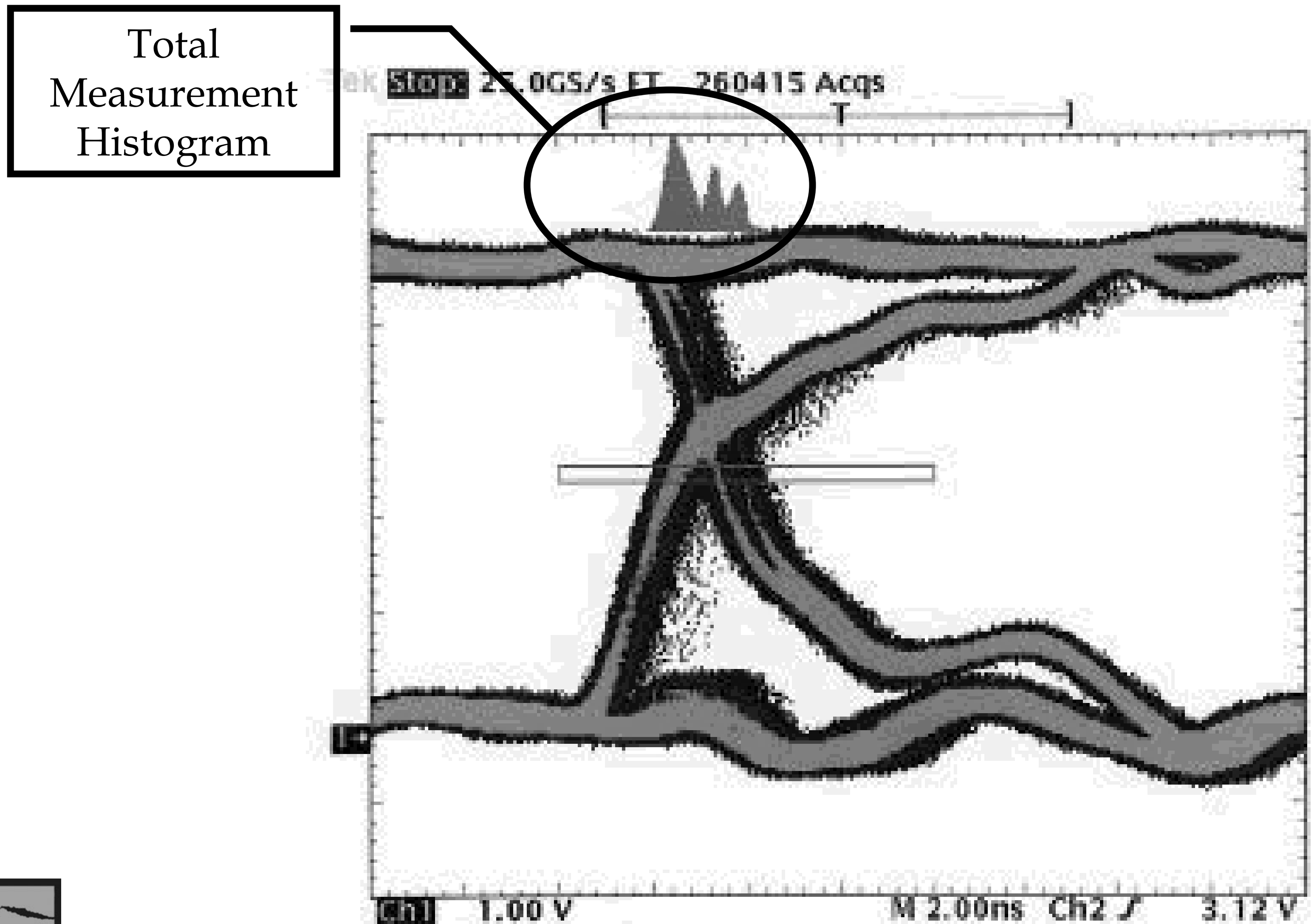
WAVECREST

July 30, 2001

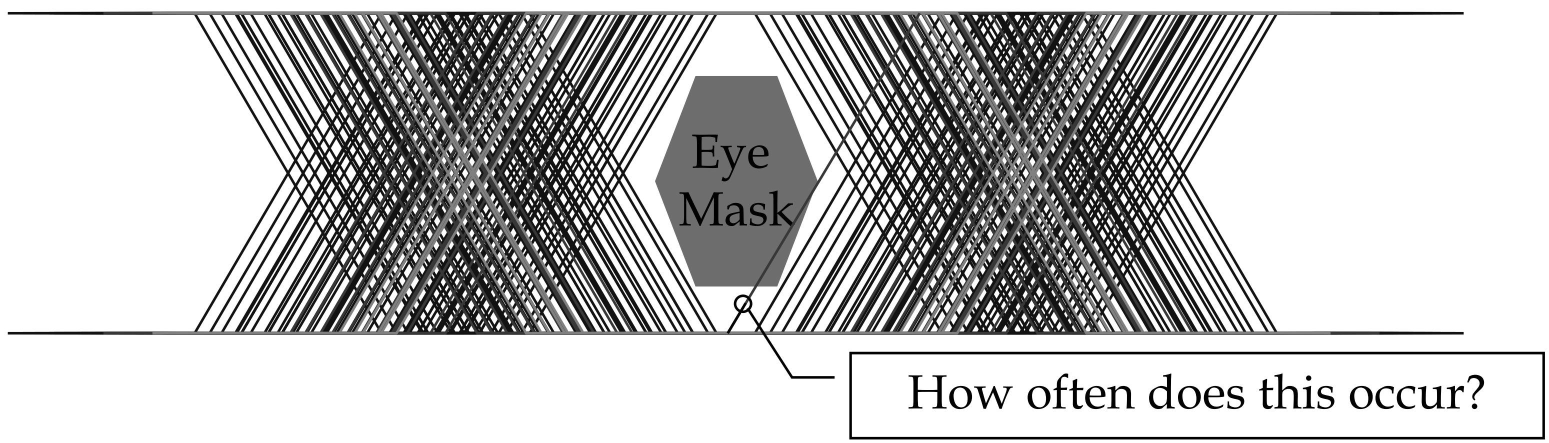
Overview of Section

- Review of Jitter components
- Why specify Jitter?
- Jitter in networks
- Introduction Jitter Specifications
- Jitter Output Testing
  - Methodologies for accurate compliance testing (FC-PY)
- Jitter Transfer Testing
- Jitter Tolerance Testing

Traditional View of Jitter on Data

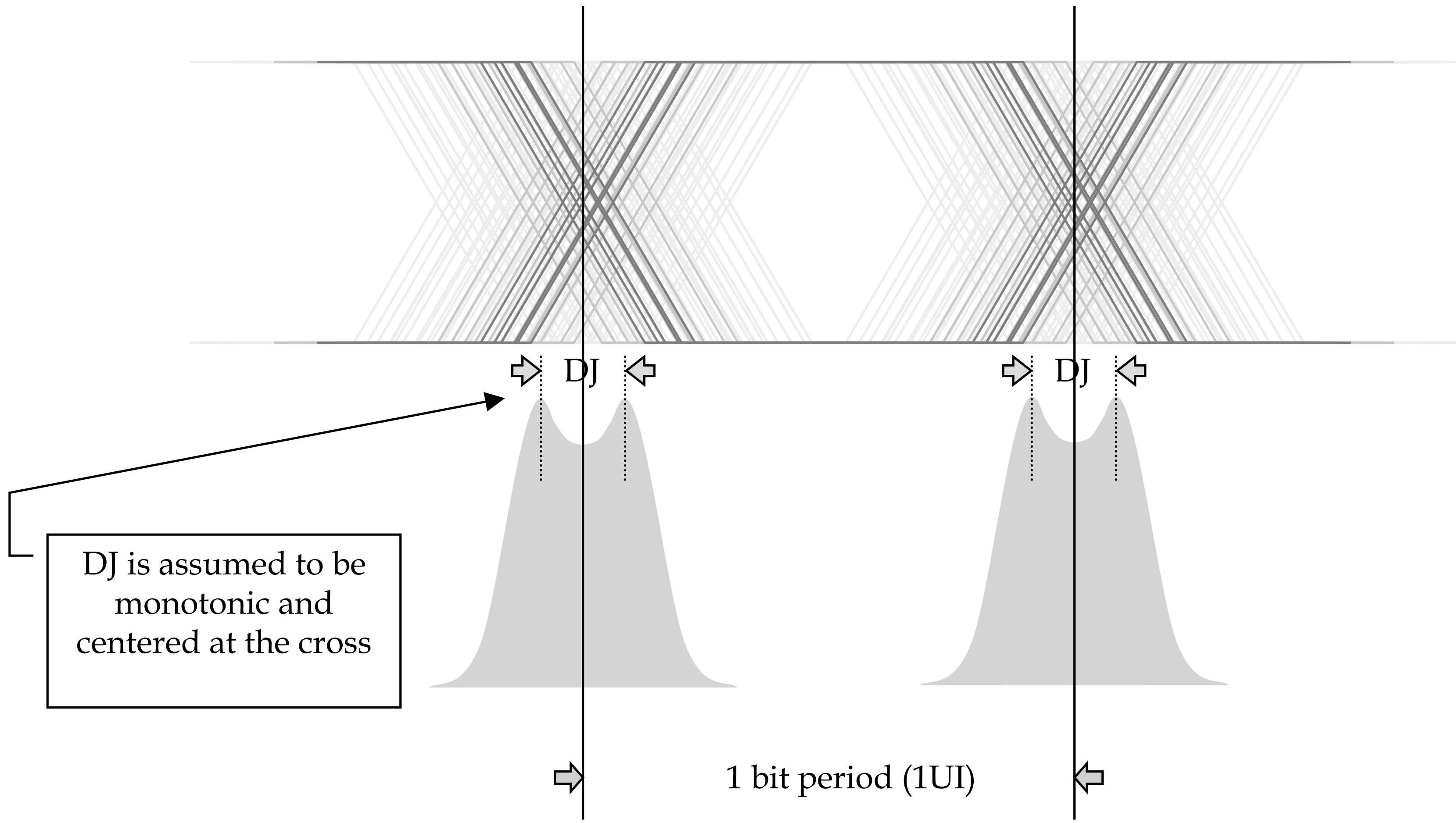


Jitter and overall BER



- Over time, Jitter causes edge transitions to encroach on eye mask.
  - Eye mask defines "Keep Out" region.
  - Downstream receiver requires certain amount of voltage and timing window to ensure accurate data recognition at any given bit.
- Use Jitter to predict outliers at boundary of eye mask

Jitter on Data Signal (with Bit Clock)



- Jitter encroaches on valid data eye. Treat overall histogram just as clock histogram for eye closure BER.
  - Use TailFit™ to calculate RJ and DJ from histogram
  - Assumes reference clock is extracted from data under test using "golden PLL"

FC - Total Jitter Calculation

(Using Golden PLL and Eye-Histogram™)

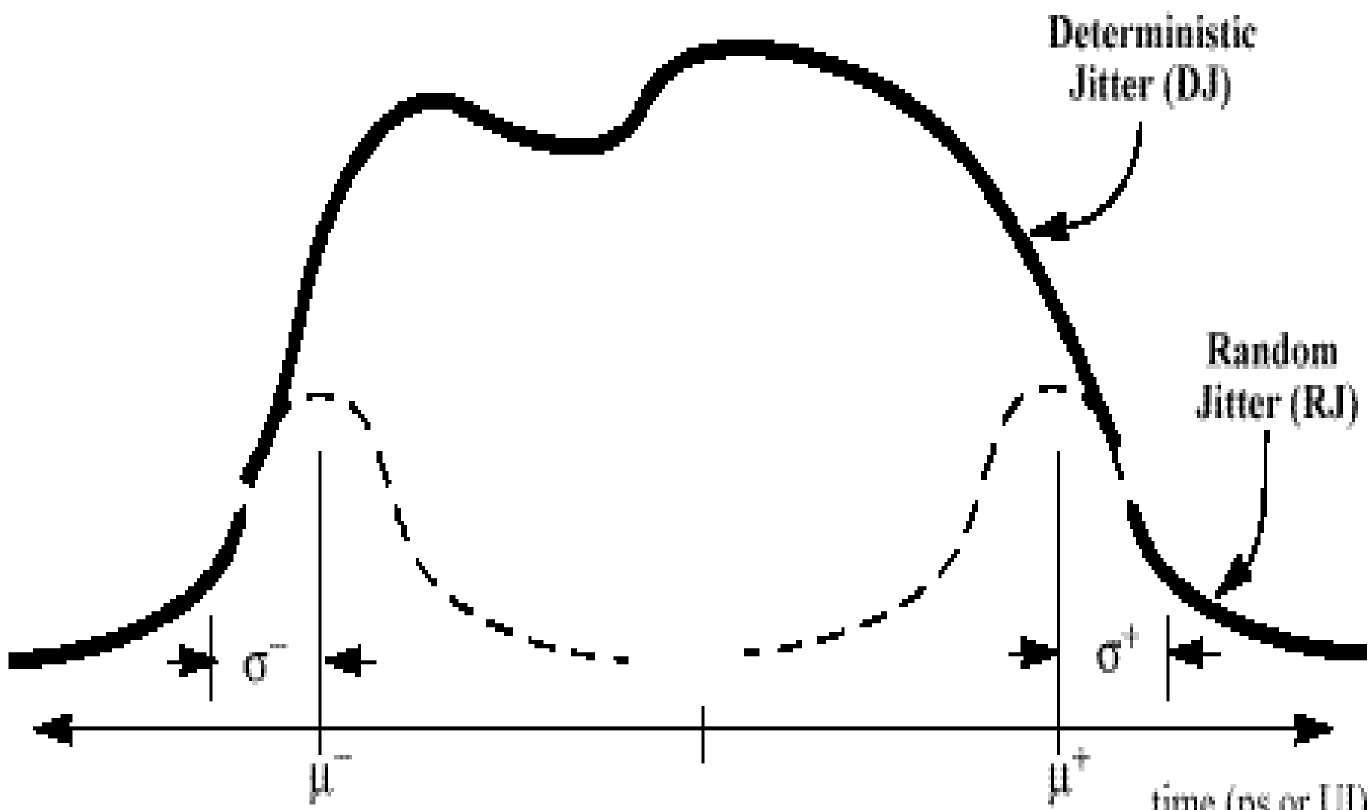
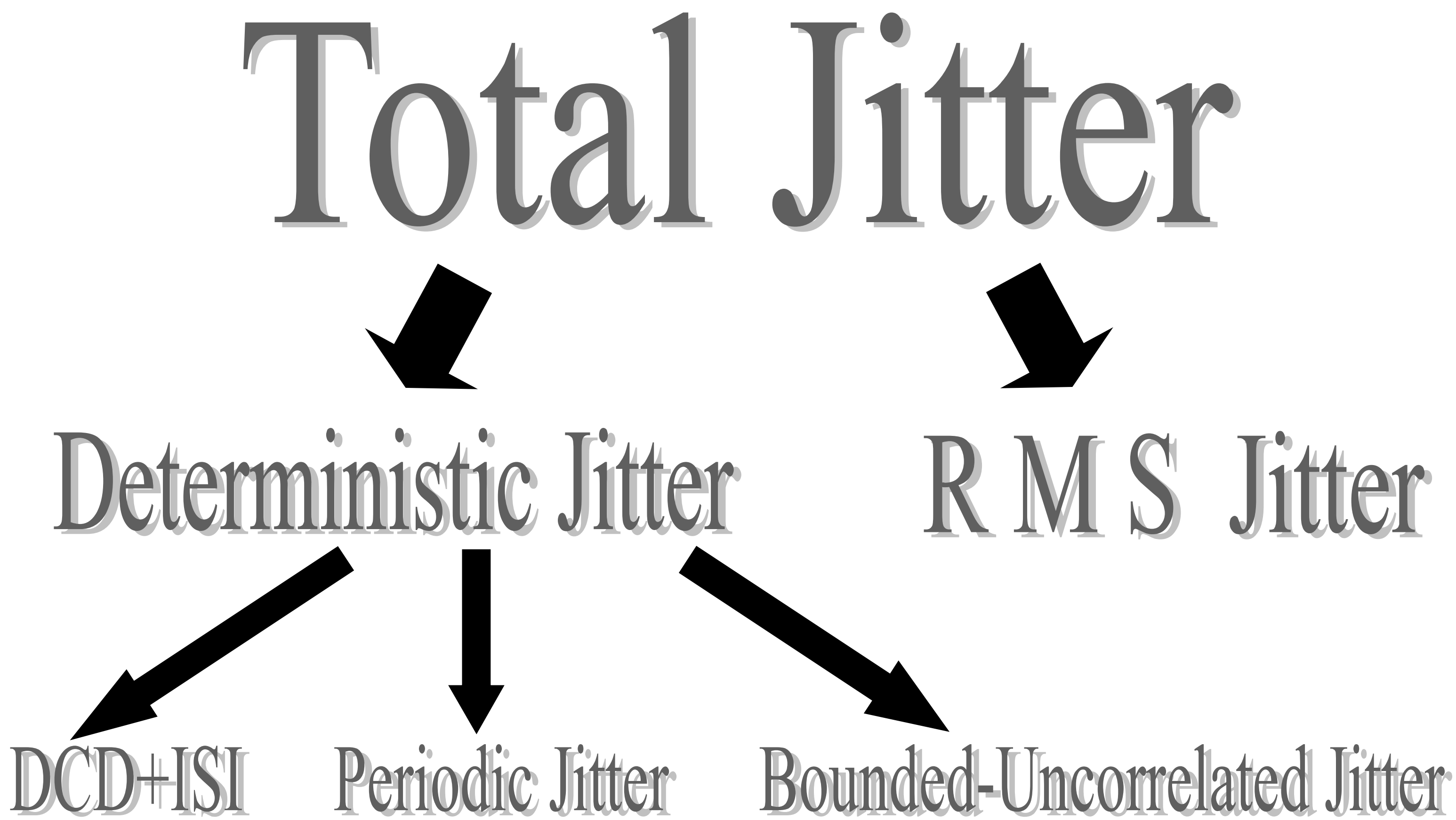


Figure D.1 – Time Domain Total Jitter Calculation

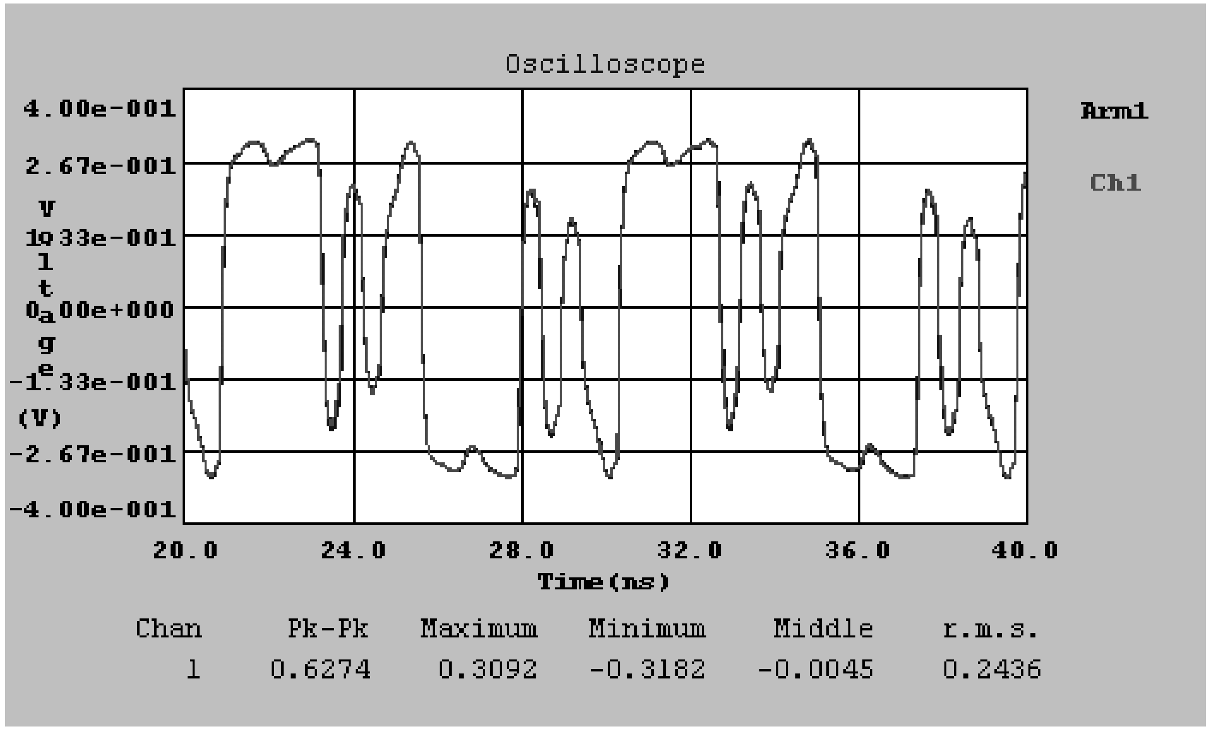
Jitter Terminology Review



Jitter Terminology Review

- Deterministic Jitter (DJ)
  - DJ is bounded and effects short term stability
  - Composed of Duty Cycle Distortion (DCD), Inter-Symbol Interference (ISI), Periodic Jitter (PJ) and Bounded Uncorrelated Jitter (BUJ)
  - DCD & ISI
    - Can quantify the quality of the interface and the Input and Output impedance matching
    - Typically caused by bandwidth limited media or driver in transmitter.
  - PJ
    - Can quantify cross talk effects from EMI sources and adjacent or nearby signal paths and quality of clock source.
    - Signals sharing media, such as in DWDM configurations or in network switches, can sometimes be susceptible to cross talk contamination. SONET switches supporting multiple standards exhibit some level of PJ at relevant frequencies.
- Random Jitter (RJ)
  - RJ is unbounded and is best described by a Gaussian distribution.
  - RJ is indicative of process impurities and Gaussian noise sources in the path of transmission.

Bandwidth and DDJ



- Data Dependant Jitter (DDJ)
  - Duty Cycle Distortion and Inter Symbol Interference are examples of data dependant Jitter
  - The picture above is an example of bandwidth effect on a serial data stream
    - Notice that the voltage amplitude is a function of the duration of the state

Extracting Bit Error Rate (BER) from Jitter

Calculating BER from Jitter

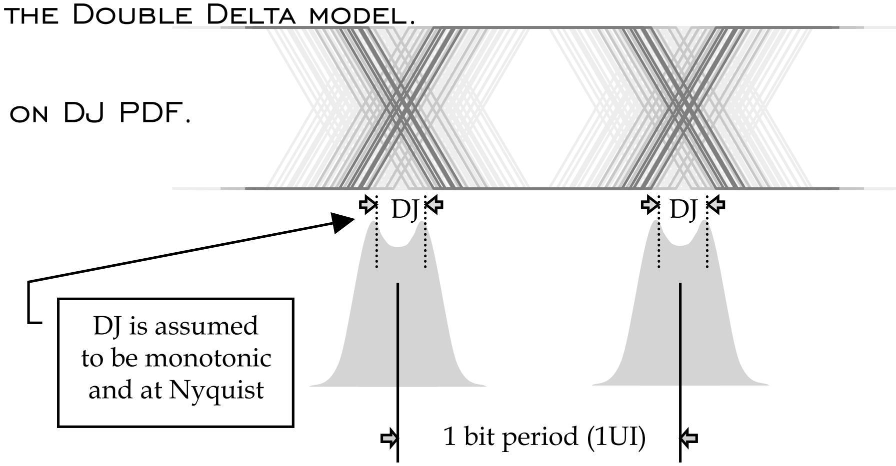
- Two Methods: (1) Easy or (2) Correct.
  - Convolution of DJ Probability Density Function (PDF) with RJ PDF
    - Requires knowledge of complete PDF.
    - PDF is a function of DJ components and their individual PDF
    - DDJ PDF is a function of the pattern. For short patterns, this can be assumed to be double poled.

$$TJ(t) = f(t) * g(t) = \int_{-\infty}^{+\infty} f(\tau)g(\tau - t)d\tau$$

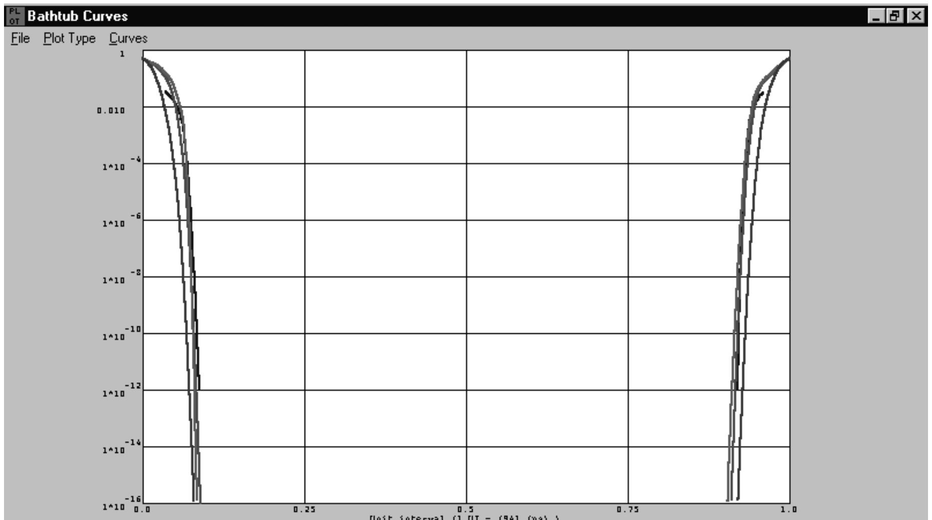
  - Simple Sum is an easy alternative in the absence of DJ PDF.
    - Some times referred to as the Double Delta model.
    - Uses simple math
    - Can over estimate TJ based on DJ PDF.

$$TJ = DJ + n \times RJ$$

Where n is the σ level desired.

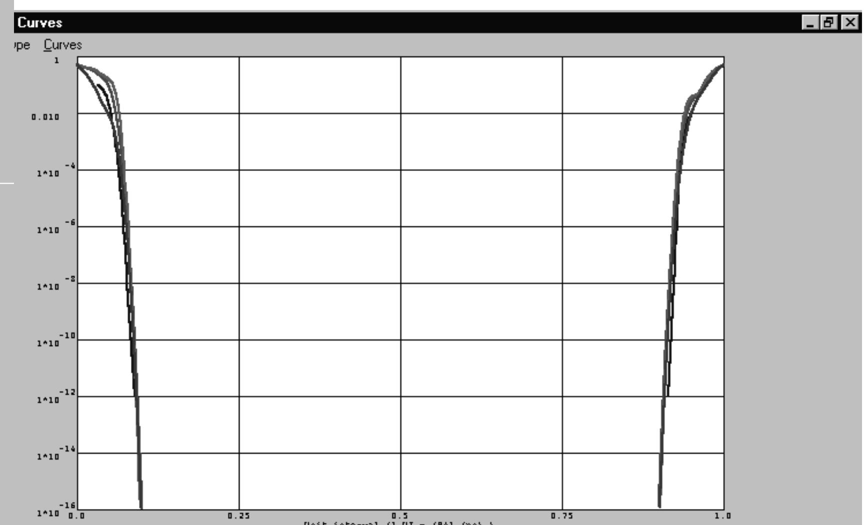


Correlating to Reality



	DCD+DDJ	PJpk-pk	DJpk-pk	RJ(1sigma)	TJ
DTS Data COM	94.668	4.273	98.942	4.569	156.865
DTS Eye Histogram					
Data - Clock			106.322	4.029	159.226
Clock			5.893	3.449	47.678
DTS No Clock/No Marker			72.042	5.193	136.059
HP BERT					157.385

- Correlation study to the left shows a 500fS difference for TJ between BERT and Eye Histogram for BER of 10^{-12}
  - This is less than a .05% error
  - Eye Histogram uses same Clock to Data relationship as BERT.
  - This Correlation Study proves the validity of the convolution method proposed in the MJS document.

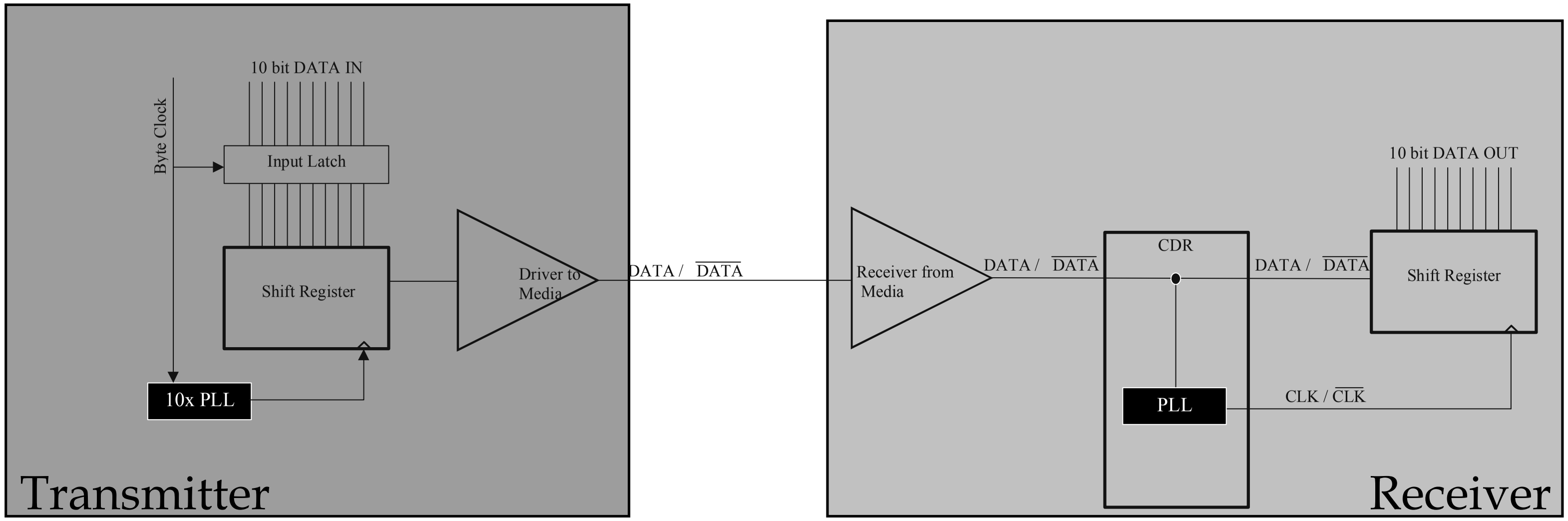


	DCD+DDJ	PJpk-pk	DJpk-pk	RJ(1sigma)	TJ
DTS Data COM	103.753	4.175	107.928	5.344	175.898
DTS Eye Histogram					
Data - Clock			109	4.762	172.041
Clock			5.726	3.382	46.444
DTS No Clock/No Marker			105.731	5.376	172.078
HP BERT					163.871

- Correlation study to the right is for PRBS 2^7-1 while the above study is for a MRPAT
  - See www.t11.org or www.wavecrest.com for further details on correlation between convolution of Jitter components and BERT

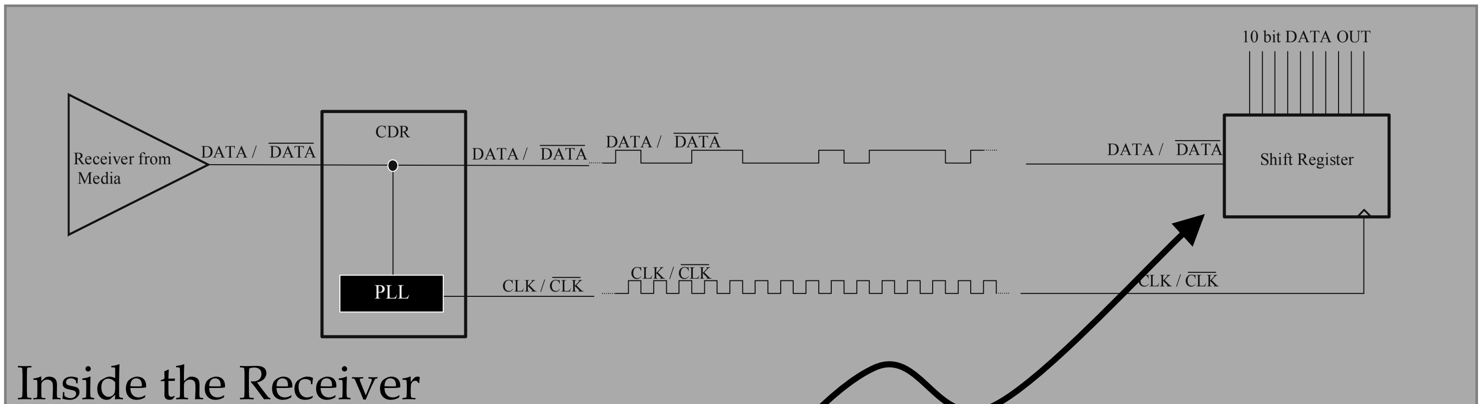
The Making of a Jitter Specification

Typical Receiver/Transceiver Pair

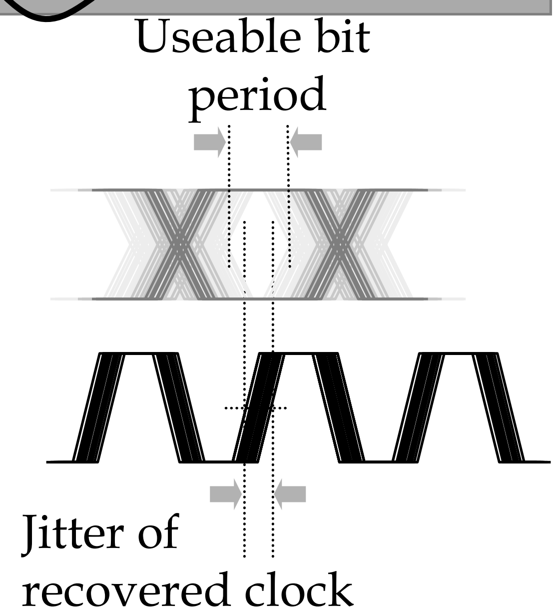


- For accurate data transmission
  - Receiver must accurately identify the data bits in the sequence they were sent.
  - Any jitter or clock timing error originating in the receiver must be accounted for in the useable bit period at the shift register.
    - The recovered clock edge in the receiver must arrive at the shift register within the useable bit period. Otherwise, the data from the wrong bit period will be captured.
  - For interoperability to be insured, proper limits leading up to the receiver must be established and adhered to.

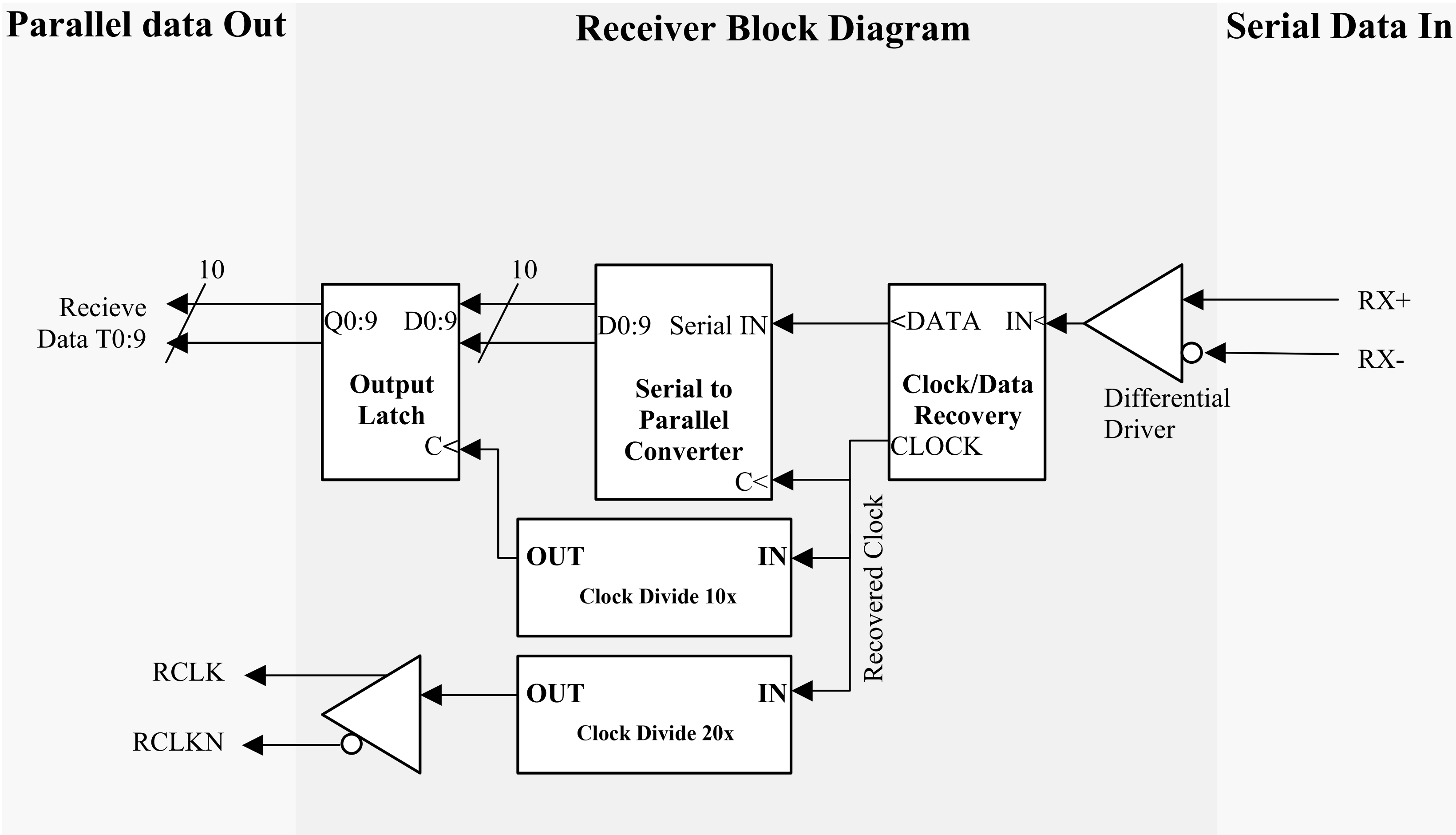
Receiver design dictates jitter component (RJ,PJ,DJ,TJ) tolerance levels



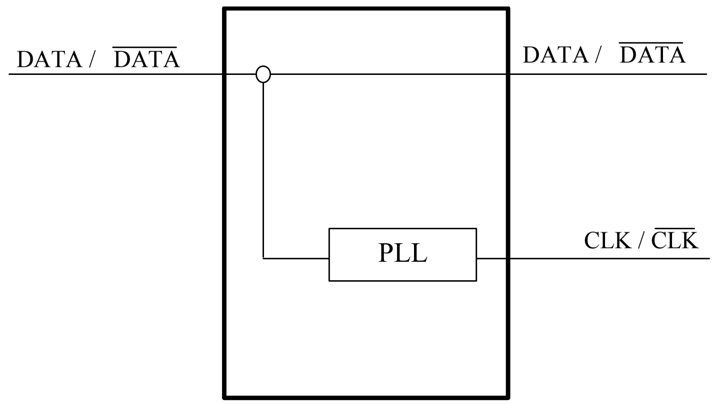
- Effect of jitter on data stream at the SERDES interface results in a reduction in the useable bit period.
- Jitter of recovered clock must fall within the remaining useable bit period.
- Useable bit period is equal to the eye opening at a desired bit error rate.



Typical Receiver Block Diagram

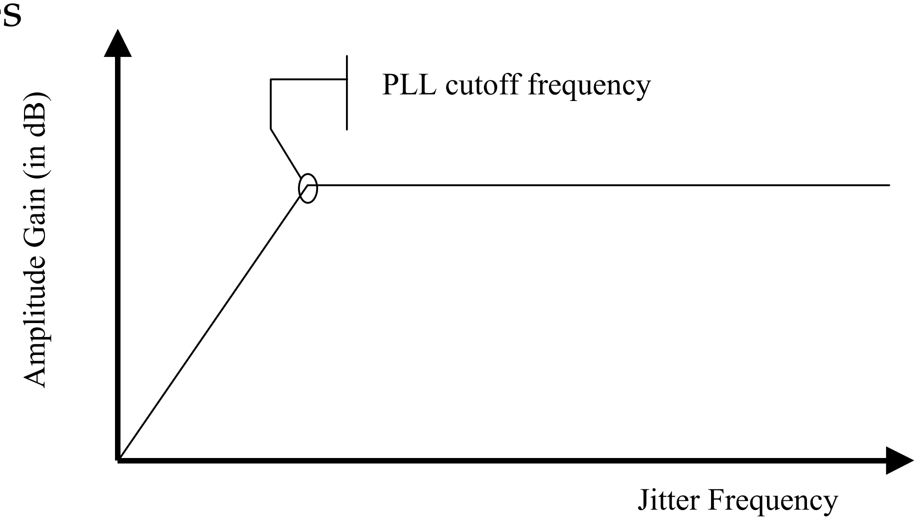


Typical Clock Data Recovery Device

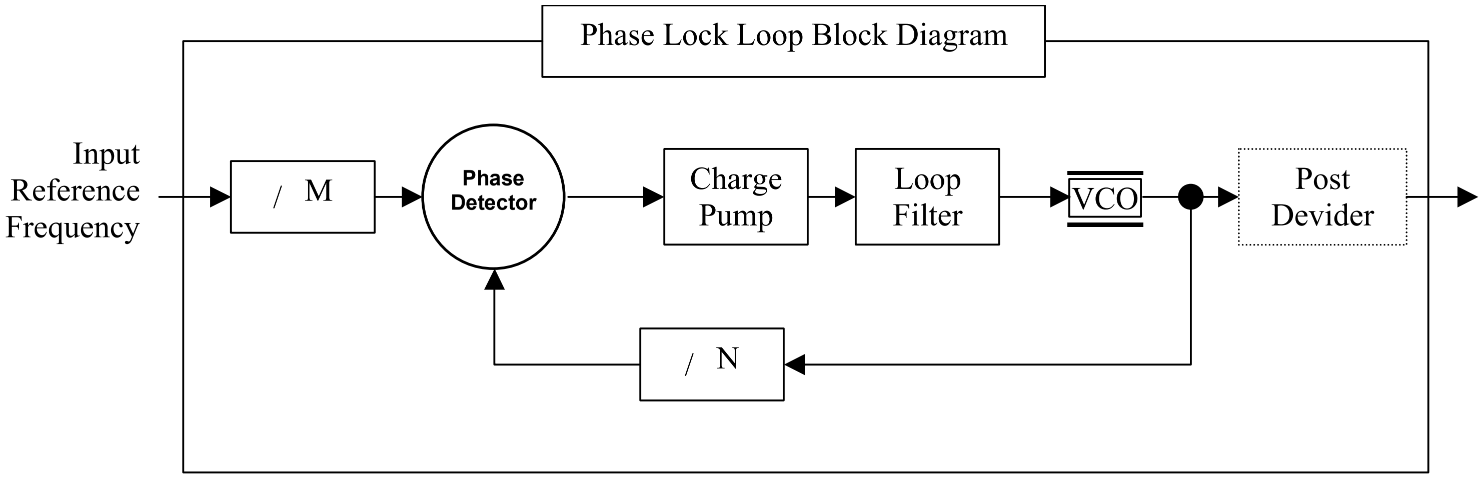


- Typical CDR composed of data pass through and clock extraction circuit (typically a PLL)
- Clock is used to trigger de-serializer
- Data is sampled by de-serializer at prescribed delay from the reference edge of clock.

- PLL in CDR has a characteristic frequency response. Frequencies below this cutoff frequency are tracked by the PLL and passed through to the de-serializer.
- Frequencies above the cutoff frequency are masked out and are not passed to the de-serializer

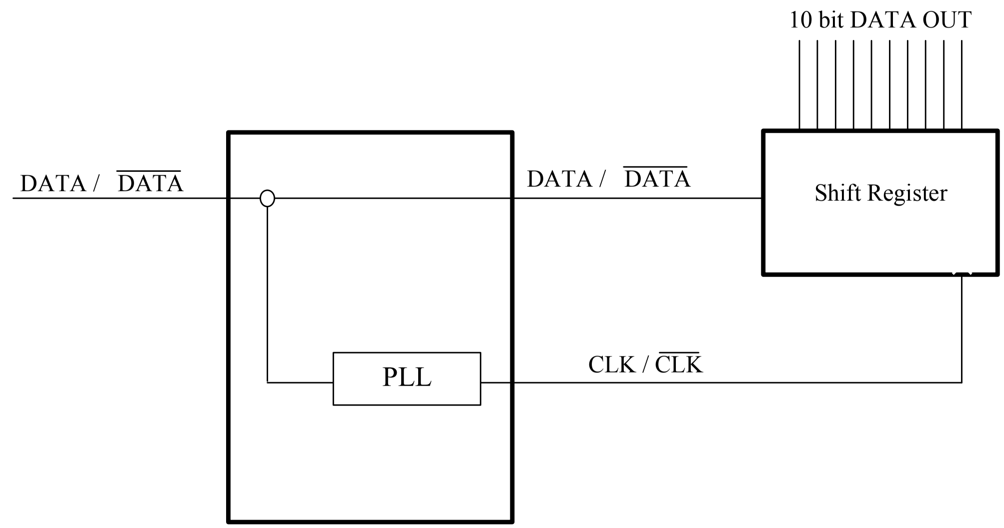


Fundamentals of a PLL



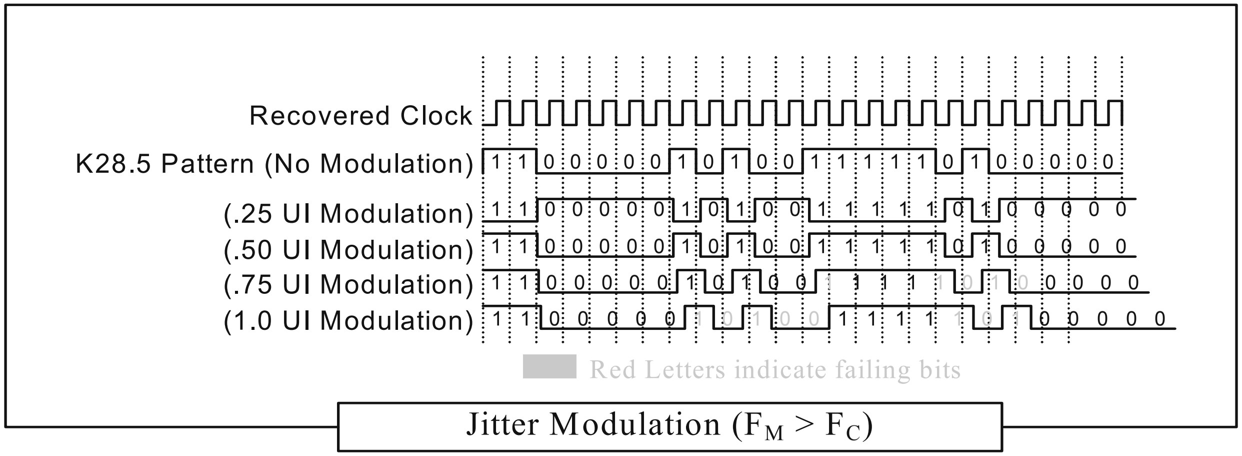
- Output Frequency = F_{REF}*P/N
  - If a Post divider is used, the output frequency is scaled accordingly
- The Charge Pump and Loop Filter are responsible for establishing the voltage on the VCO thereby establishing the output frequency of the VCO.
  - VCO voltage is established based on the phase and frequency relationship of the feedback loop and the input reference frequency.
- The loop response of the PLL is a function of the loop response through the feedback divider (N).
  - Loop response of the PLL defines the low frequency cutoff detection of the receiver in which it is used. Low frequency cutoff in a receiver is that modulation frequency below which modulation will not effect eye opening.

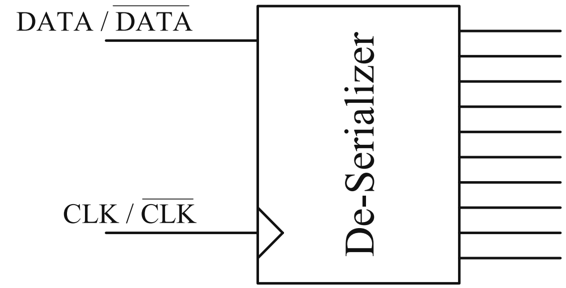
How Jitter Affects Receiver



- All jitter on the data stream is fed into shift register (de-serializer)
- High frequency jitter (Jitter Modulation above F_C) is filtered off of clock signal. (PLL is not tracking it.)
- Recovered clock is used to latch data in Shift Register.
- Jitter between recovered clock and data can cause the wrong data to be latched in the shift register.
- Bandwidth limiting effects resulting in ISI Jitter on data will not be observed on the recovered clock.

Effect of PJ on De-Serializer





- For Periodic Jitter Frequencies above the PLL cutoff frequency, De-Serializer may not capture the accurate data.
  - Data will still have the modulation component adjusting the time at which the transition occurs.
  - Clock signal will have filtered out the modulation since it cannot track the modulation frequencies above it's cutoff frequency.
- THEREFORE: Jitter Specifications are defined in terms of amplitude and frequency.

Fundamentals of Jitter Specification

- Jitter Specifications start with defining the performance of the Receiver. Useable bit period at the receiver is the fundamental metric for performance.
- TJ Specification
  - The TJ budget dictates the amount of useable bit period available to the receiver.
    - Useable Bit Period (Eye Opening) = Bit Period – TJ@BER
- PJ Specification
  - Magnitude of periodic Jitter is dependant on frequency of modulation.
    - Cutoff frequency of PLL in receiver dictates the low frequency modulation tolerance of the receiver.
    - Maximum Amplitude of PJ component above CDR-PLL cutoff is a function of total DJ tolerance of the given interface. Various governing bodies establish limits for total DJ over a given frequency band.
- RJ Specification
  - Magnitude of RJ is based on the Total Jitter at a given Error Rate.
    - TJ is essentially the inverse of the useable eye opening at a given error rate. Since TJ is composed of both RJ and DJ, governing boards must decide adequate limits for at least TJ.

Examples of Jitter Specification

- Fibre Channel –
  - We will use Fibre Channel MJS specification as an example of data signal jitter specification. Other protocols use different methodologies for specifying the same thing. Namely, useable bit period at the deserializer of the receiver.
    - SONET, for example, uses a combination of spectral peaks and RMS of jitter within various frequency bands. This technique is very time consuming and requires quite specific test setups to properly measure jitter compliance. Each setup is specific for a given frequency band and for specific bit rates.
      - Traditional SONET test methods require the analysis of the recovered clock. This can be very difficult to do without a "golden PLL" for accurate clock regeneration.
      - SONET ATM and packet switched VoIP are currently competing for protocol dominance in the >10Gbps arena. Which ever protocol wins will probably establish the telecommunication standards for many years to come.
      - SONET standards and methodologies are addressed in a separate telecom jitter training jitter module.
  - Fibre Channel compliance for jitter is established through maintaining specific DJ and TJ limits at various points along the communication path known as "Compliance Points."
  - Note: much of the MJS rev 10 specification is focused on the 1.0625Gbps speed. See the relevant ANSI specification for other protocol limits.

Compliance Points

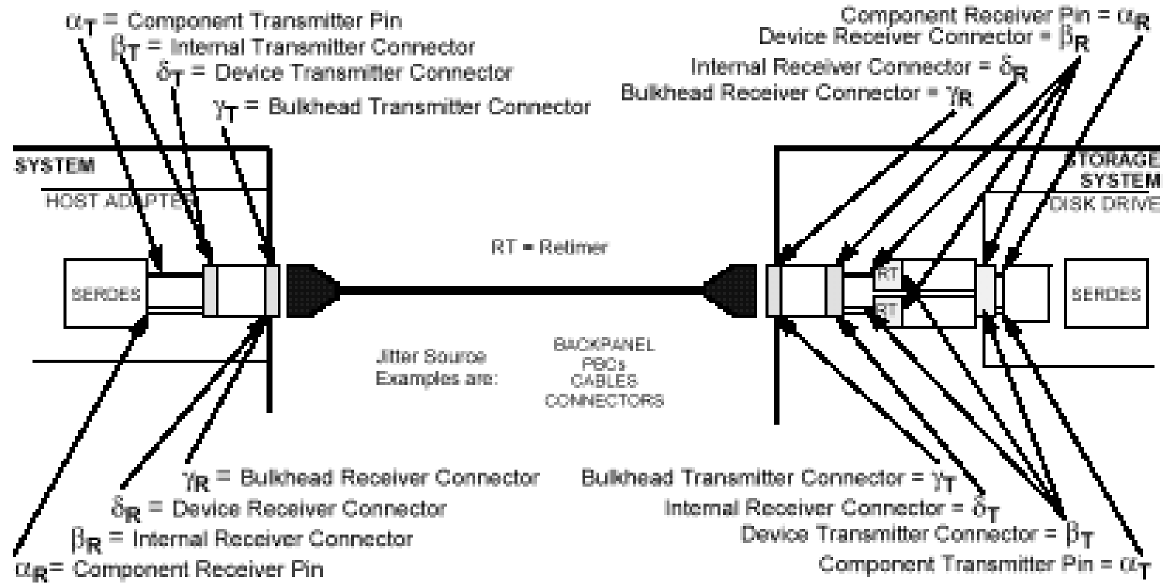


Table 6 – 1,0625 GBaud jitter output allocation (Passband of 637 kHz to greater than 5 MHz)

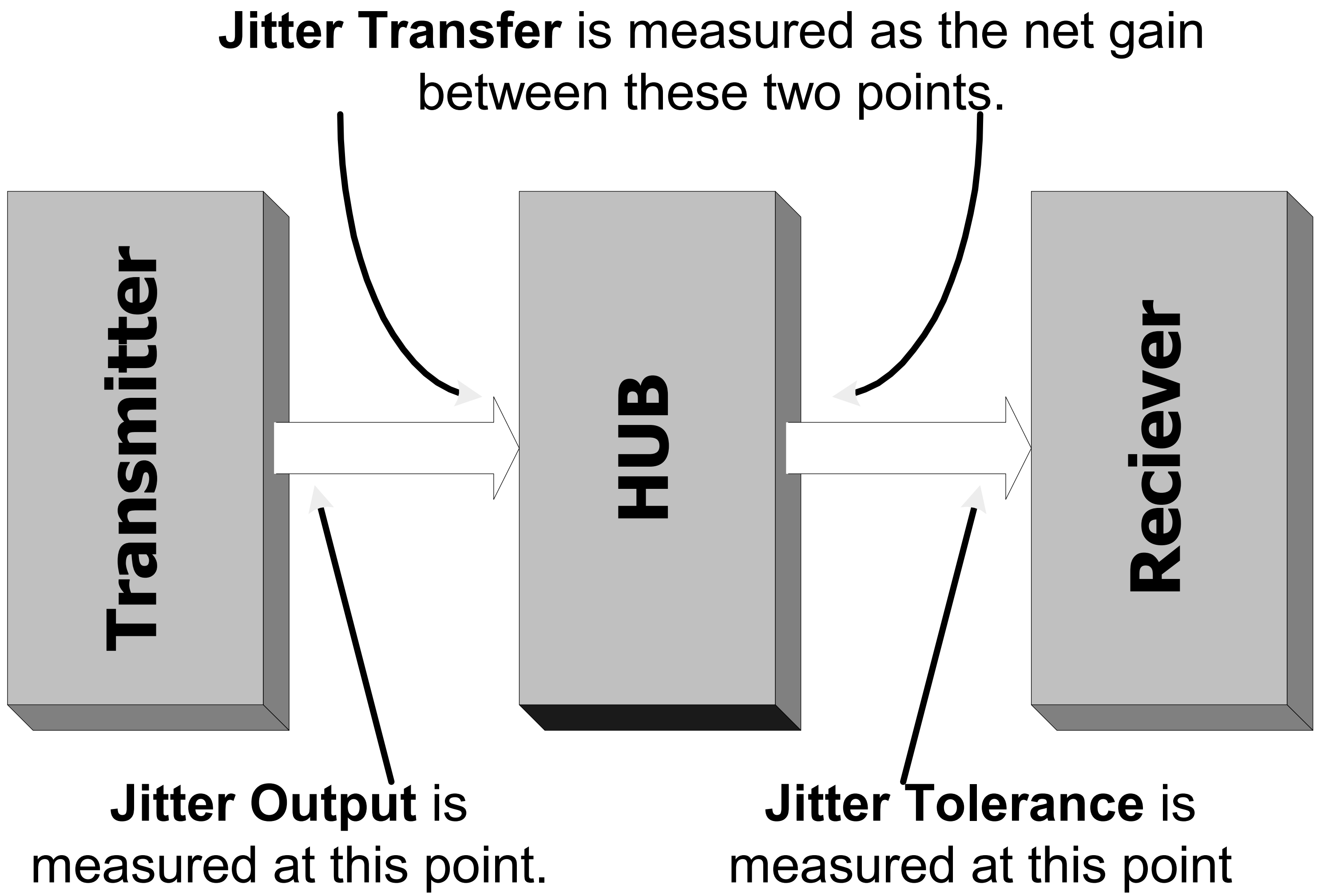
Variant	Jitter (Unit Interval - UI)								
	Component	α_T	β_T	δ_T	γ_T	γ_R	δ_R	β_R	α_R
100-SM-xx-x (single mode)	DJ Total	0,10 0,21	0,11 0,23	0,12 0,25	0,21 0,43	0,23 0,47	0,36 0,61	0,37 0,63	0,38 0,65
100-Mx-xx-x (multi-mode)	DJ Total	0,10 0,21	0,11 0,23	0,12 0,25	0,21 0,43	0,24 0,47	0,36 0,61	0,37 0,63	0,38 0,65
100-xx-EL-x (copper)	DJ Total	0,10 0,21	0,11 0,23	0,12 0,25	0,13 0,27	0,35 0,54	0,36 0,56	0,37 0,58	0,38 0,60

Fundamentals of Jitter Testing

Jitter Output (Generation),

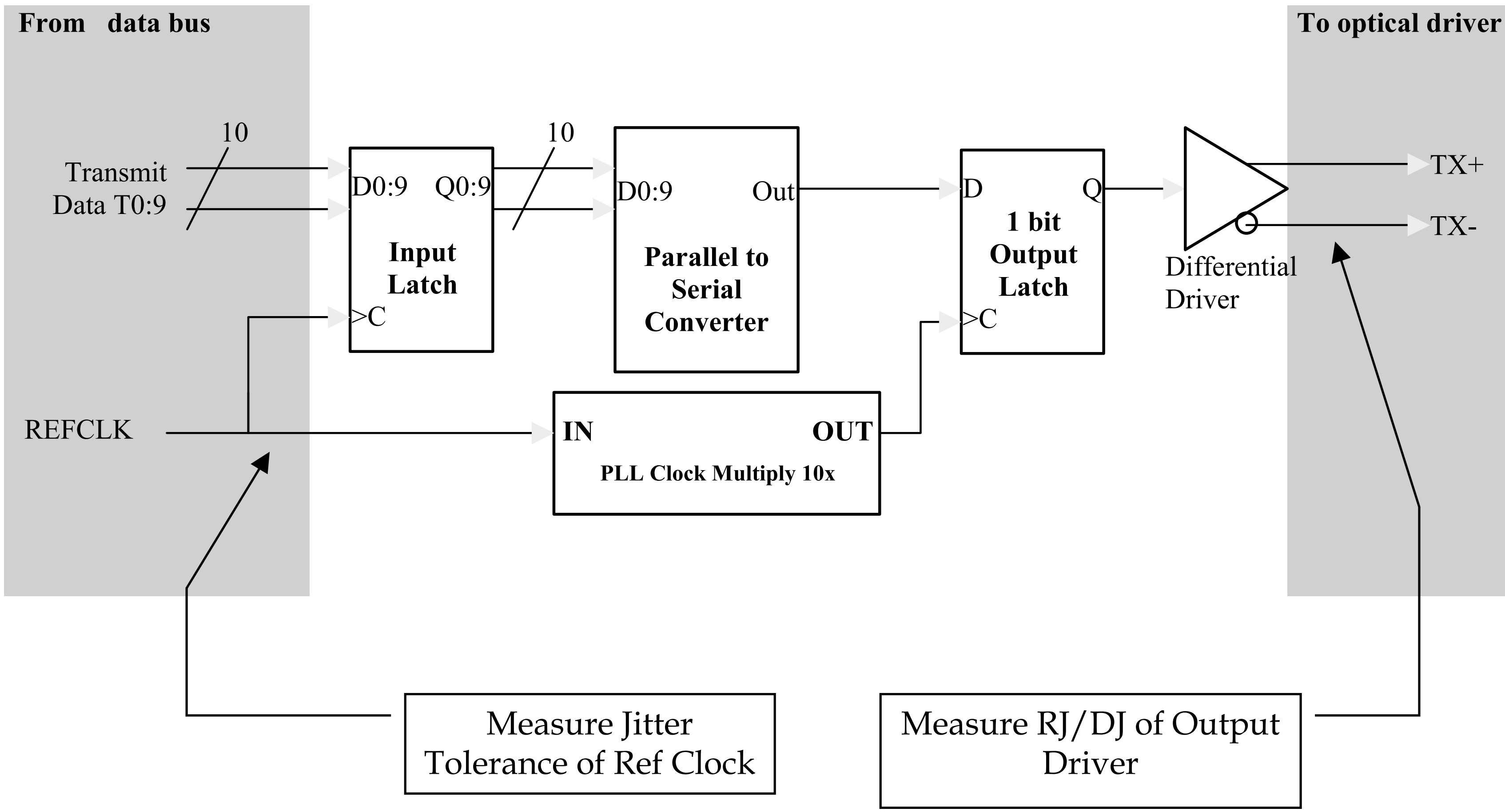
Jitter Transfer and Jitter Tolerance

INTRODUCTION TO JITTER

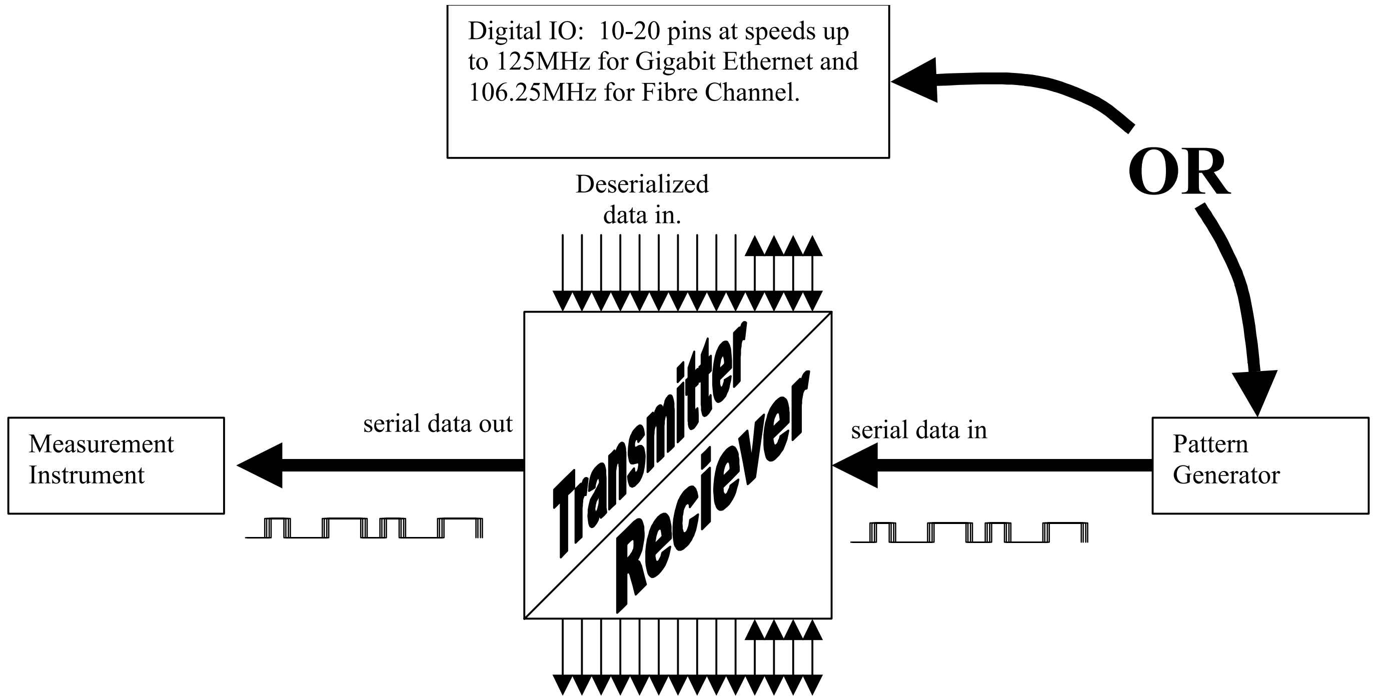


Jitter Testing of Transmitter

Typical Transmitter Block Diagram

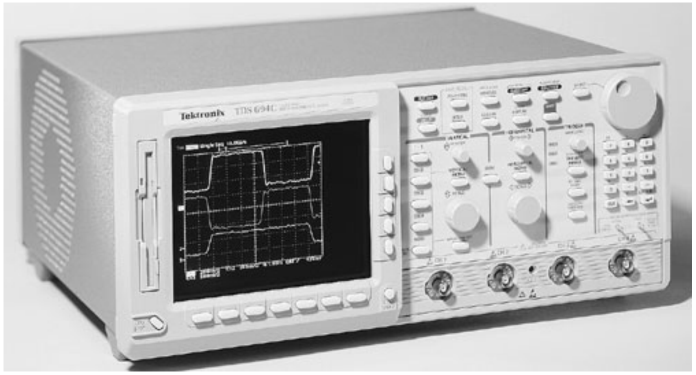


How to Connect

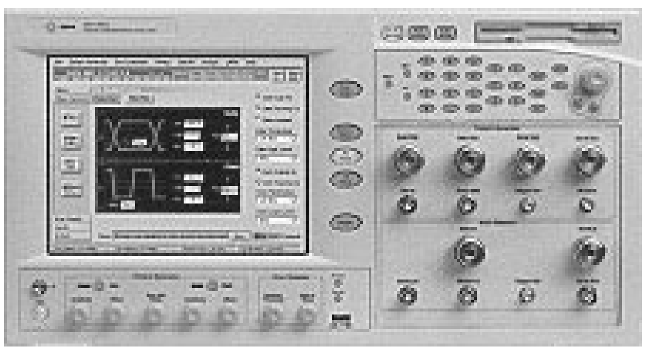


- Set control bits to allow data transfer from either Receiver in (bypass mode) or from Transmitter buffers.
  - Use looping pattern
  - Provide pattern marker (for Wavecrest)
  - Provide golden PLL for compliant CDR (for BERT or O'scope)

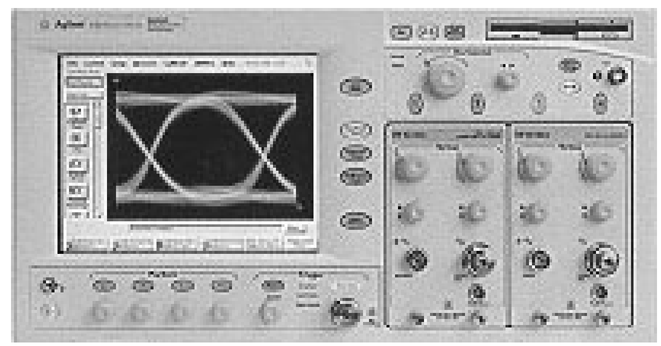
POSSIBLE SOLUTIONS



Cannot use a Digitizing Oscilloscope

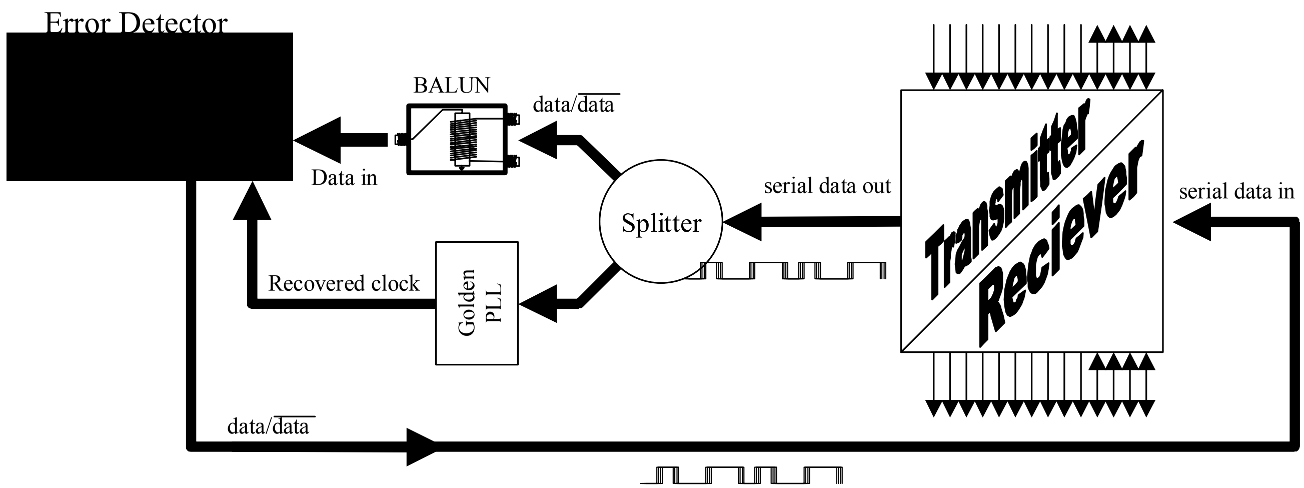


(with FC compliant CDR(Golden PLL) for triggering)



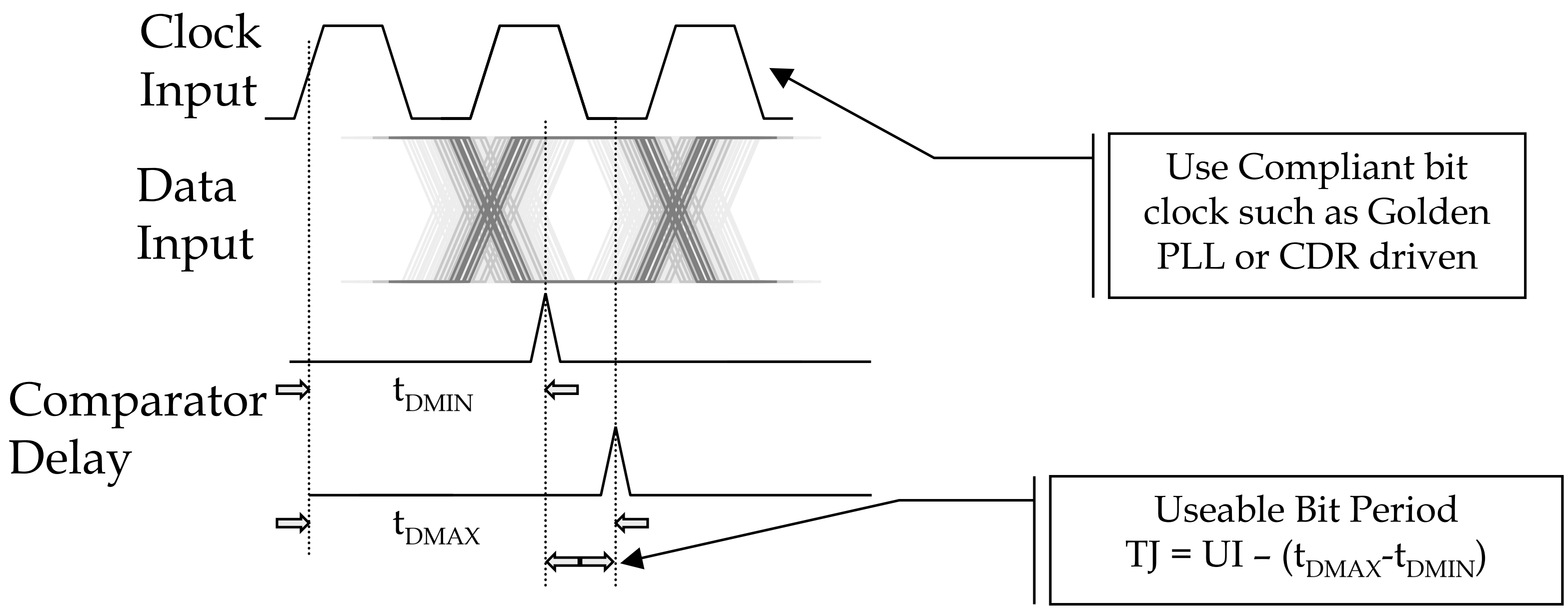
(with FC compliant CDR(Golden PLL) for triggering)

Using a BERT



- Bit Error Rate Tester (BERT)
  - Requires Golden PLL (compliant CDR with specified frequency response characteristic)
    - For Fibre Channel, this would be a PLL with a loop response of 637kHz
  - Using BERT's clock for data triggering could cause false readings
    - Clock is synchronous with data
    - May mask periodic components originated in test equipment or may not mask PJ components which are acceptable (below F_C)

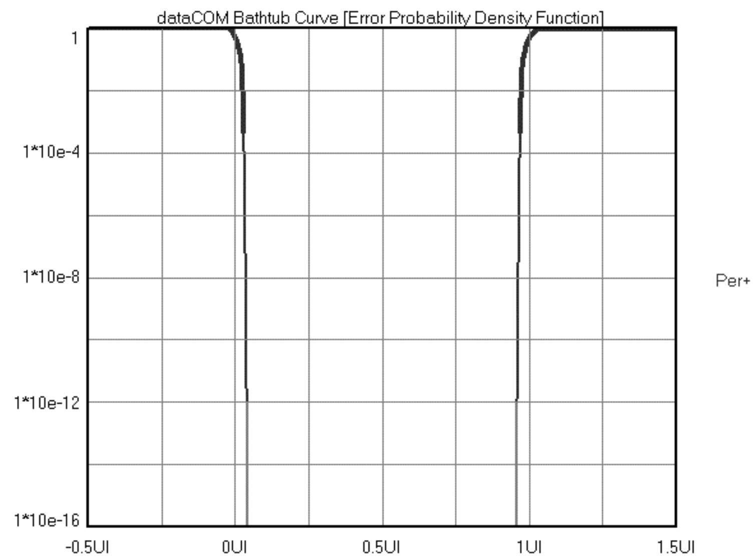
Using the BERT for Total Jitter Measurement



- Bit Error Rate Test (BERT) Systems
  - Adjust Comparator delay to find t_{DMAX} and t_{DMIN} for bit error rate (BER) in question (14σ for Fibre Channel Compliance)
  - Subtract (t_{DMAX}-t_{DMIN}) from Unit Interval (UI) to get Total Jitter (TJ) at given BER
  - Be sure to execute through entire reliability level desired (for 14 σ reliability, test at least 10^{12} cycles of data)
    - for Fibre channel, each pass = 941.7 seconds (@1Gbps)
    - may take several passes to find pass/fail boundary

Result = Total Jitter

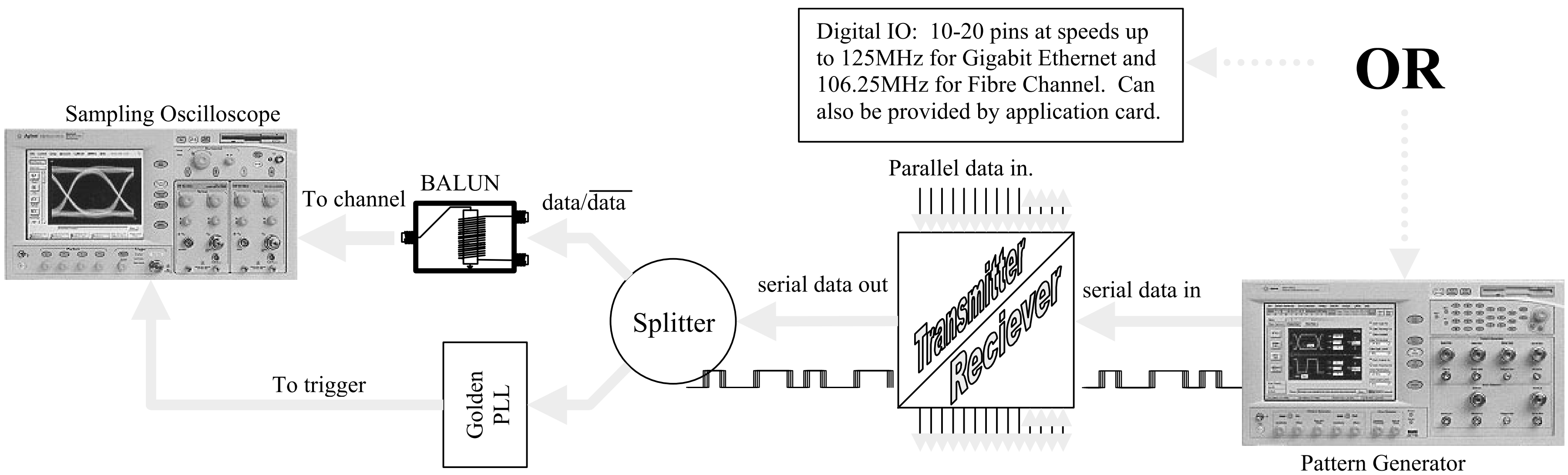
Developing Bathtub curve from BERT data



- Bathtub curves show TJ versus Error Probability
  - Can be generated from BERT data based on TJ values and the associated BER with the TJ level
  - BERT should not be used for high BER areas of Bathtub curve
    - RJ/DJ de-convolution is impossible without time domain relationship information of DJ components and RJ component
    - Use BERT based bathtub curve only for BER above 10^{-6}
  - If no low occurring DJ is present, TJ can be extrapolated from BERT bathtub curve
    - Obtain TJ data for BERs of 10^{-6}, 10^{-7}, 10^{-8}, and 10^{-9}. Then extrapolate curve to 10^{-6} for TJ at 14σ

See www.wavecrest.com for a correlation study of using this method.

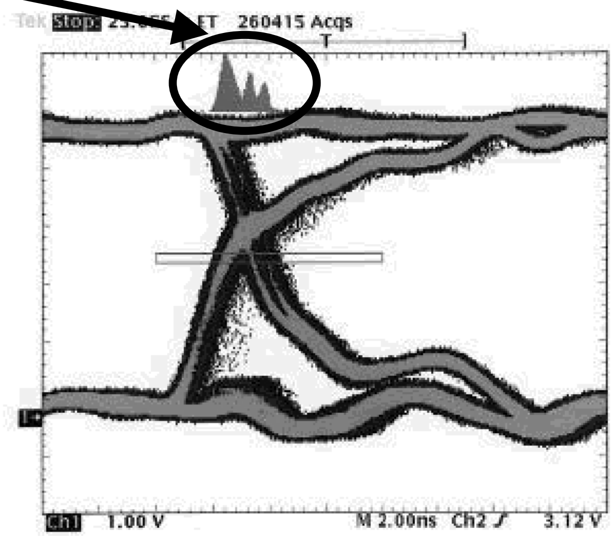
Using Sampling Oscilloscope

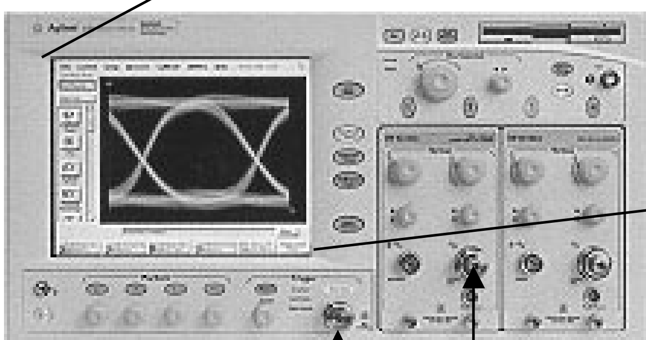


- Sampling Oscilloscope measures clock to data jitter
  - Since the measurement is triggered against the clock signal, the jitter measurement is actually the clock to data jitter. This may or may not be representative of the actual jitter on the data stream.
    - In order to best approximate the result, be sure use a golden PLL.
  - Jitter Result will be Total Jitter peak to peak. No Jitter Separation available for oscilloscopes.
  - Number of hits is inversely proportional to desired BER. Therefore, be sure to take enough data to display 10^{12} hits at the transition point. (On many scopes, this will take several hours, so, only do this during after hours!)

Oscilloscope's View of Jitter on Data

Total Measurement Histogram



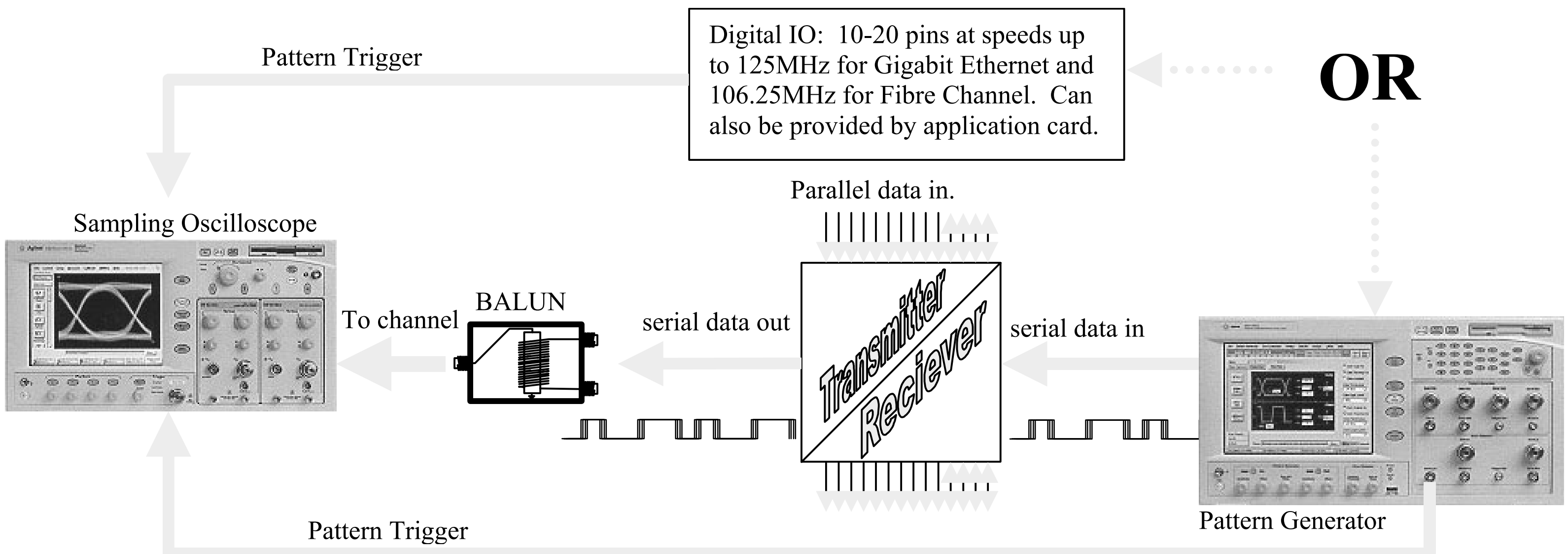


Single Ended Data Stream

Recovered Clock

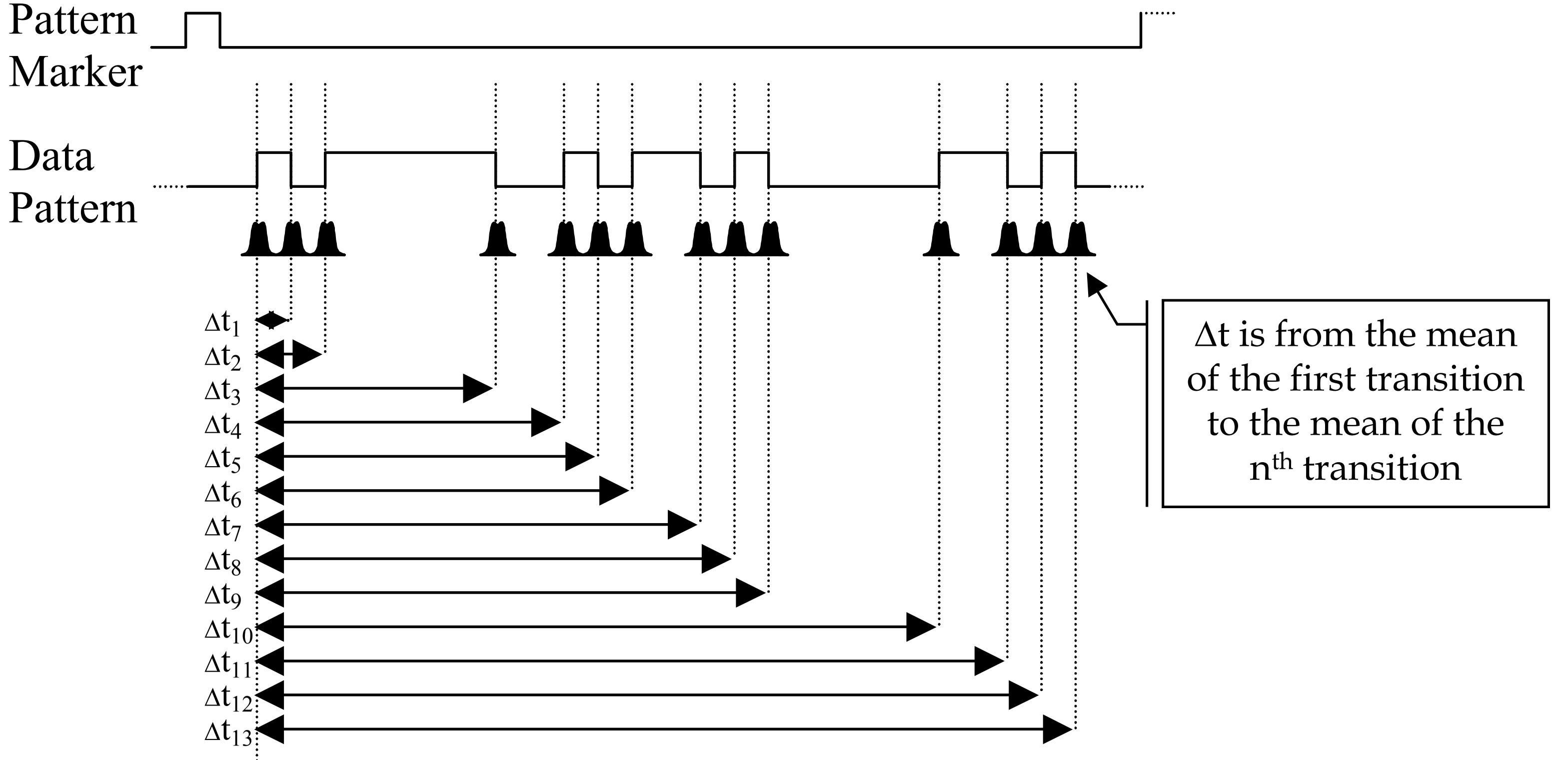
- This Histogram shows the relationship of the recovered clock to the data stream. This is not the jitter on the data.
- Keep in mind that the scope delay may mask high frequency components.

Using the O'scope for DDJ



- Data Dependant Jitter
  - The Sampling Oscilloscope is ideal for Data Dependant Jitter testing on data patterns less than 1024 bits long.
    - Time base drift will adversely affect accuracy on time measurements above 1 μs. Oscilloscope time base stability varies from scope to scope. Check with your scope vendor for details.
  - Trigger Oscilloscope on Pattern Marker instead of bit clock for clear picture of each transition.
  - Take enough points such that at least 500 hits occur at each transition point

Data Dependant Jitter with Oscilloscope

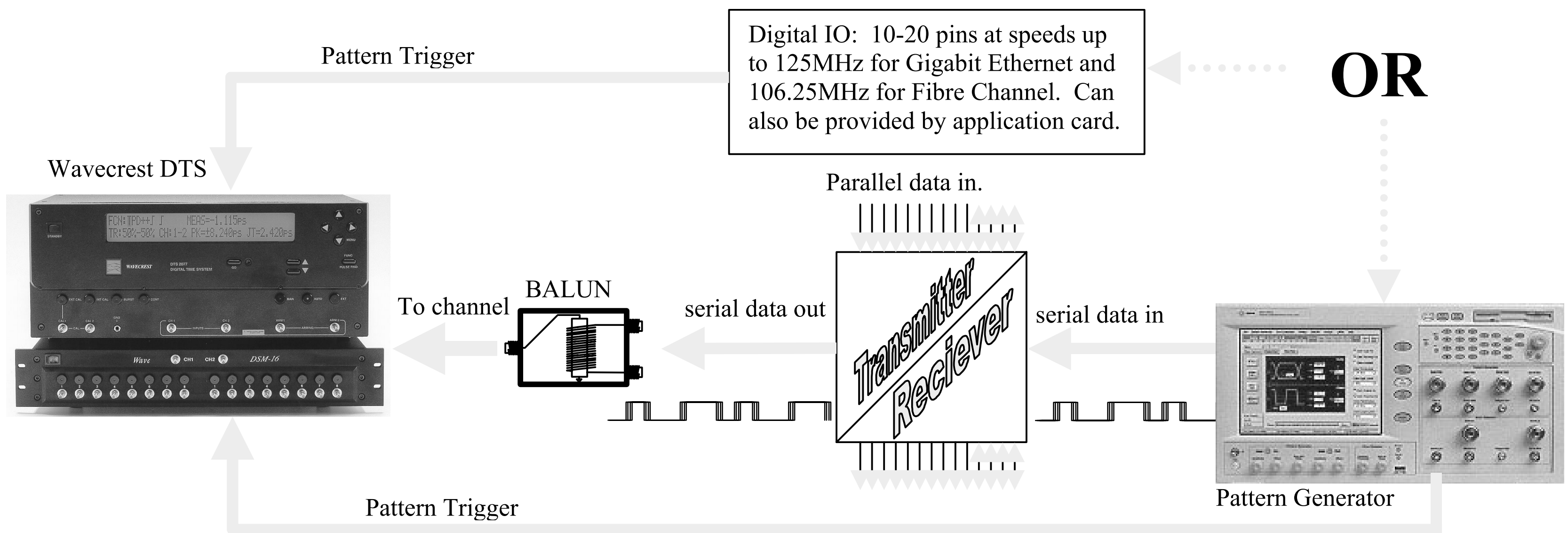


- Data Dependant Jitter (DDJ) is worst case off set of mean from ideal as follows:

$DDJ_N = \Delta T_N - m \times UI$ (where m = number of bit periods included)

$DDJ = \text{Maximum } DDJ_N - \text{Minimum } DDJ_N$

Using Wavecrest DTS to Analyze Jitter

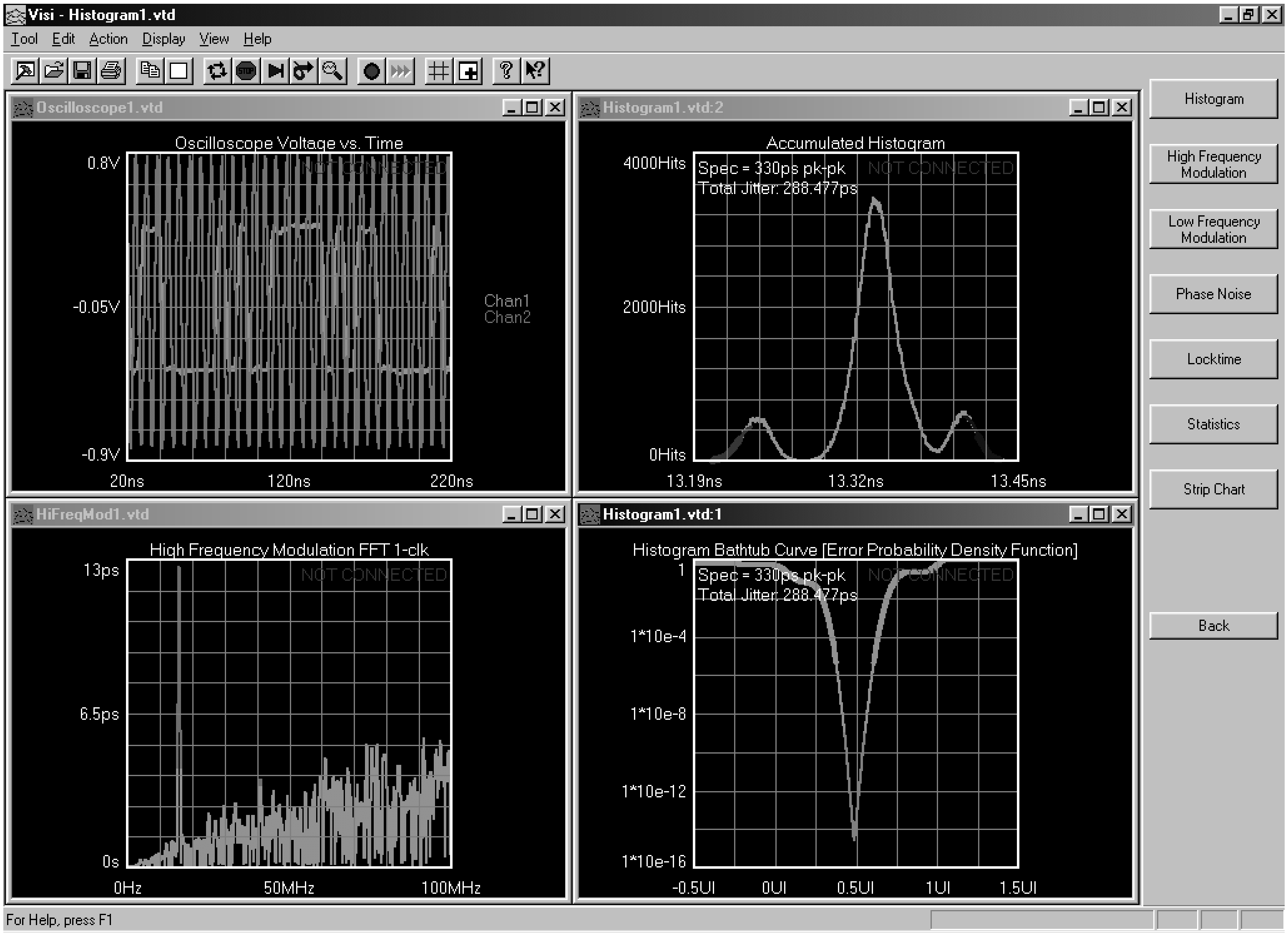


- Separation of Jitter Components
  - RJ, DCD+ISI,PJ and BUJ
- Quick Correlation
  - Laboratory, Production and Customer Application Card
  - Share Setup files and data files to compare various setups
  - Minimize operator setup error
- Characterize PLL Bandwidth and Loop-Feedback Response Time

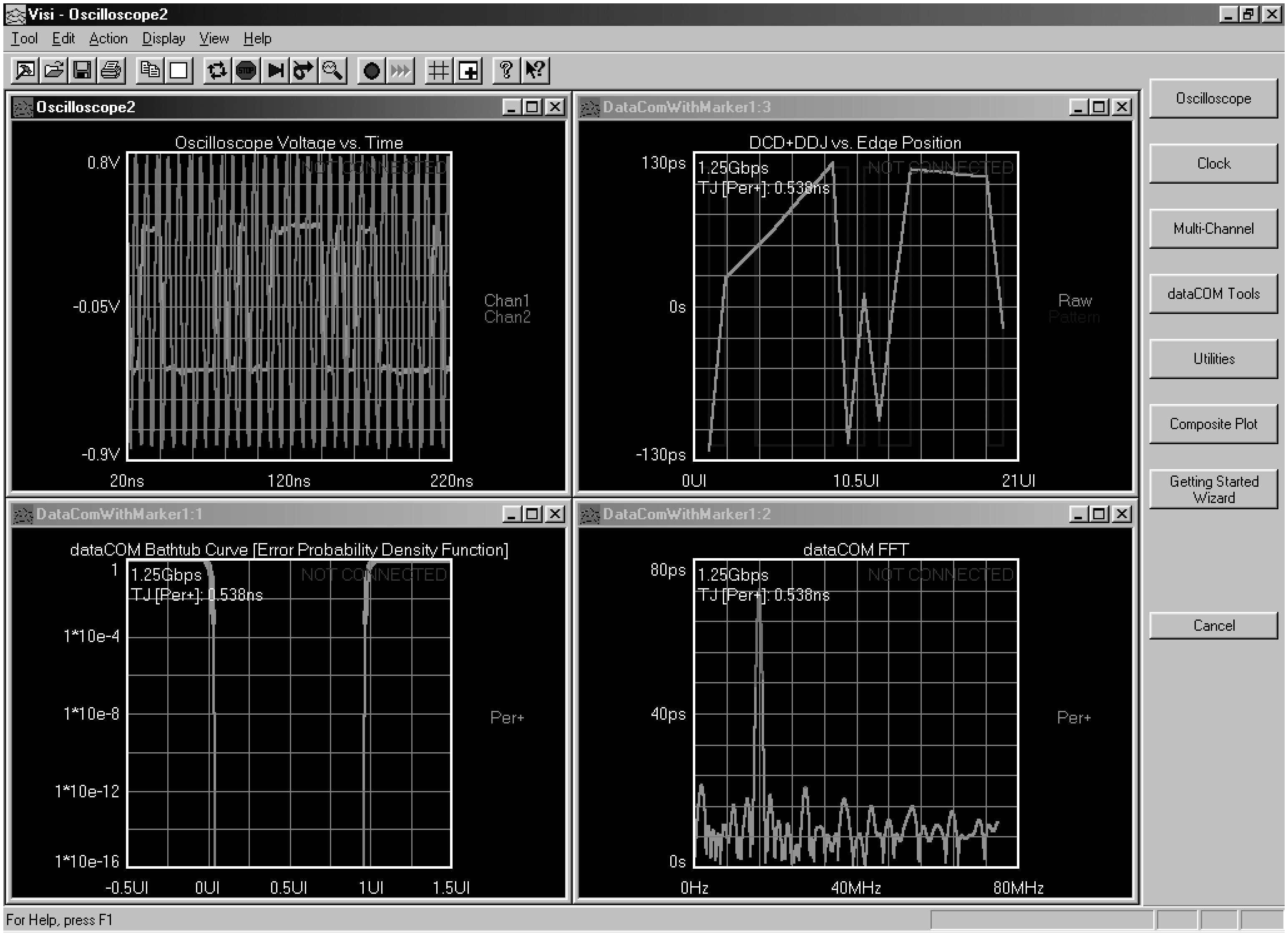
Wavecrest's VISI Toolset

(And now a word from our sponsor...)

Clock Jitter Analysis



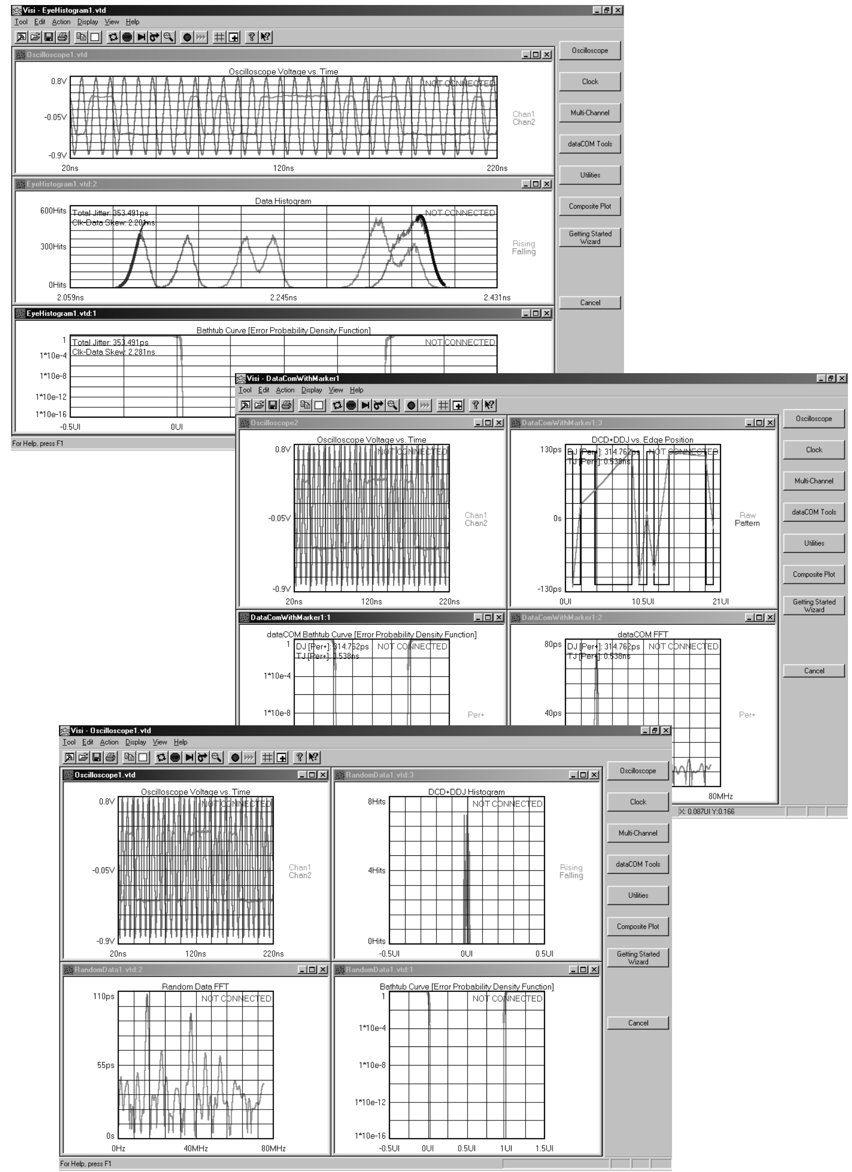
dataCOM Tools



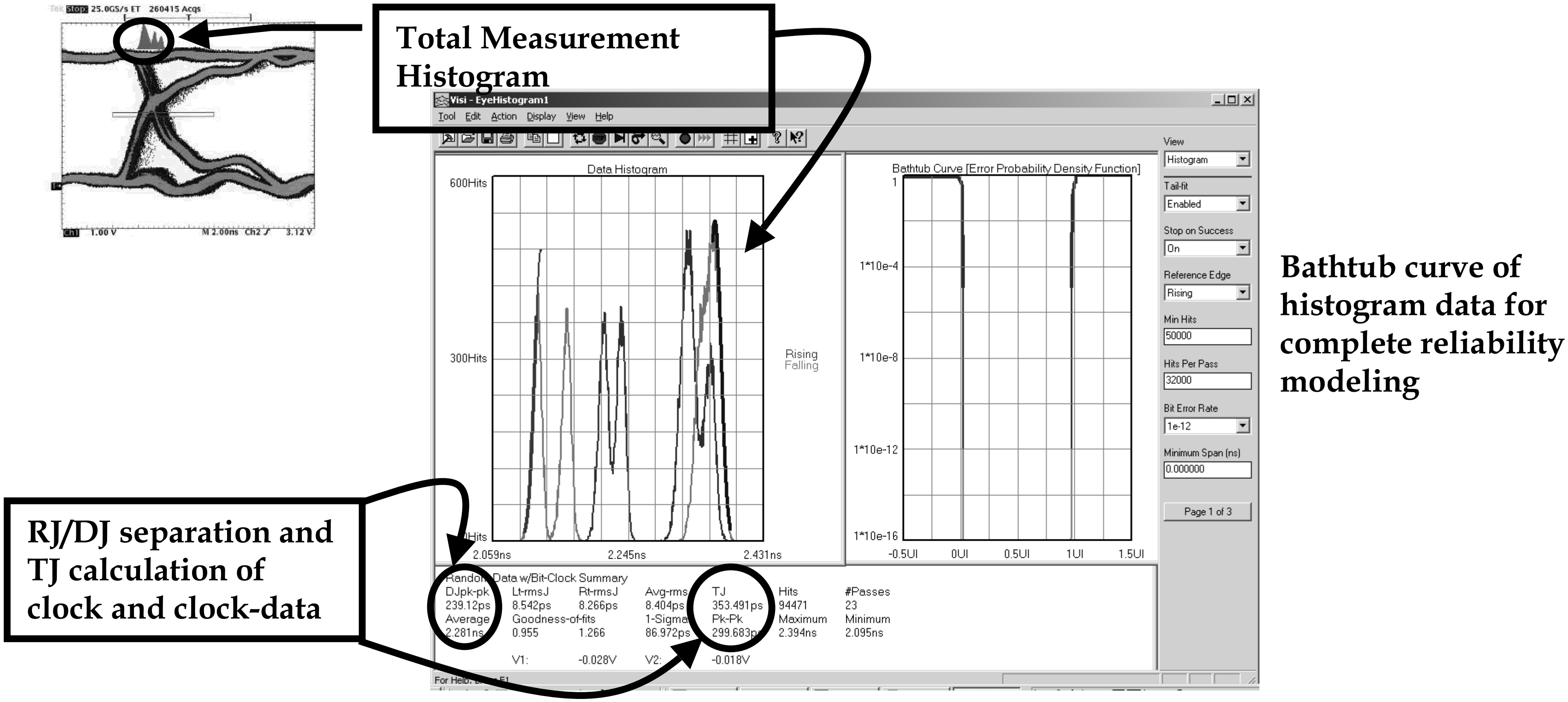
How do the VISI tools work?

What are the dataCOM tools?

- Eye Histogram
  - Analyzes "Clock to Data" Jitter just like a BERT or oscilloscope but gives the user true DJ/RJ separation for full compliance testing in record time.
- dataCOM
  - Analyzes jitter on JUST the data with the compliant filter functions already incorporated
  - Test to compliance and debug the root cause of jitter all in one tool.
- Random Data Tool
  - Analyze jitter on data without any knowledge of the data stream
  - Analyze jitter on live networks, active Fibre Channel links and scrambled disk drive data.

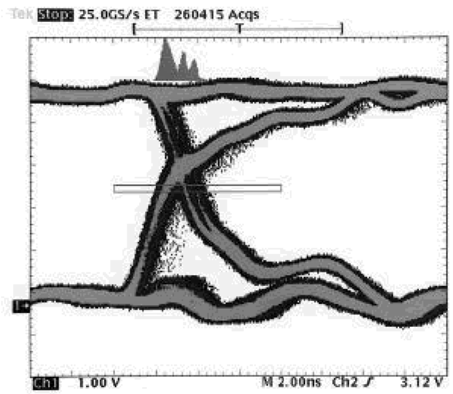


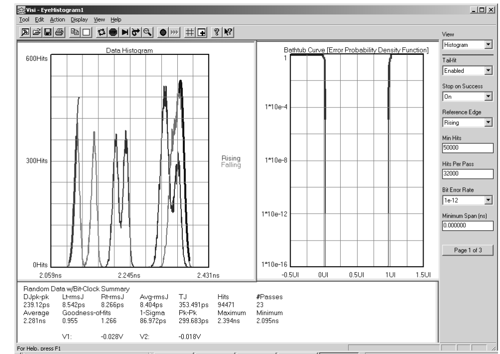
A NEW LOOK AT EYE DIAGRAMS



- EYE HISTOGRAM TOOL TAKES TRADITIONAL EYE DIAGRAM TO A NEW LEVEL
  - SAME "CLOCK TO DATA" JITTER AS THE OTHER TOOLS.
  - NO TRIGGER DELAY
  - DJ/RJ SEPARATION FOR EASY CALCULATION OF TJ
  - BATHTUB CURVE FOR EASY CORRELATION WITH BERT.
  - ANALYZE RISING EDGES SEPARATE FOR FALLING EDGES.

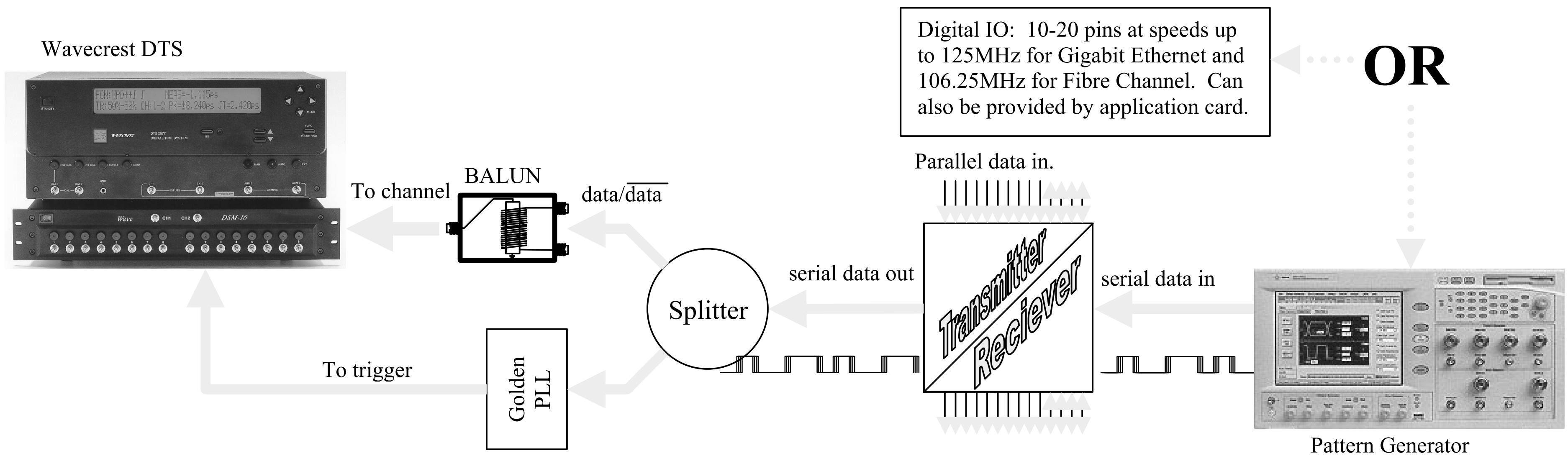
Eye Diagram vs. Eye Histogram





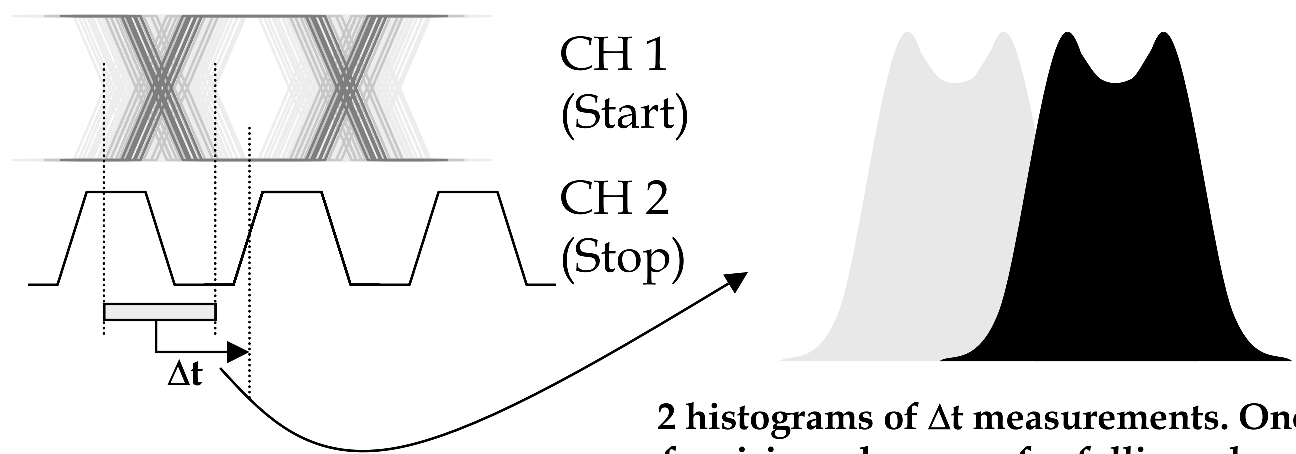
- Eye Diagram is ideal for voltage vs. time analysis
  - Use Eye Diagram for verifying voltage level stability, over shoot ringing, and other voltage based measurements
- Not a good tool for Jitter Measurement
  - No Jitter Separation
  - TJ estimate of clock to data jitter takes several hours to accumulate enough data to make a proper estimate
  - Not ANSI compliant.
- Eye Histogram gives great jitter information
  - DTS is a Time measurement instrument, therefore, time measurement is second to none.
  - VISI algorithms give complete RJ/DJ separation for accurate reliability modeling and ANSI compliance testing.
- Eye Histogram is not an Oscilloscope.
  - Use VISI Oscilloscope Tool for voltage vs. time relationship

Equipment Setup of Eye Histogram



- Set up is the same as an Oscilloscope Eye Diagram
  - Use compliant PLL as clock source (just as in o'scope) for better frequency response modeling
  - No need for delay lines (DTS does not have a trigger delay)
  - Use BALUN and 50% threshold crossing as channel input.
- Clock signal is connected to channel 2 and data signal is connected to channel 1
  - This results in a data to clock measurement.

How is the Measurement Made?

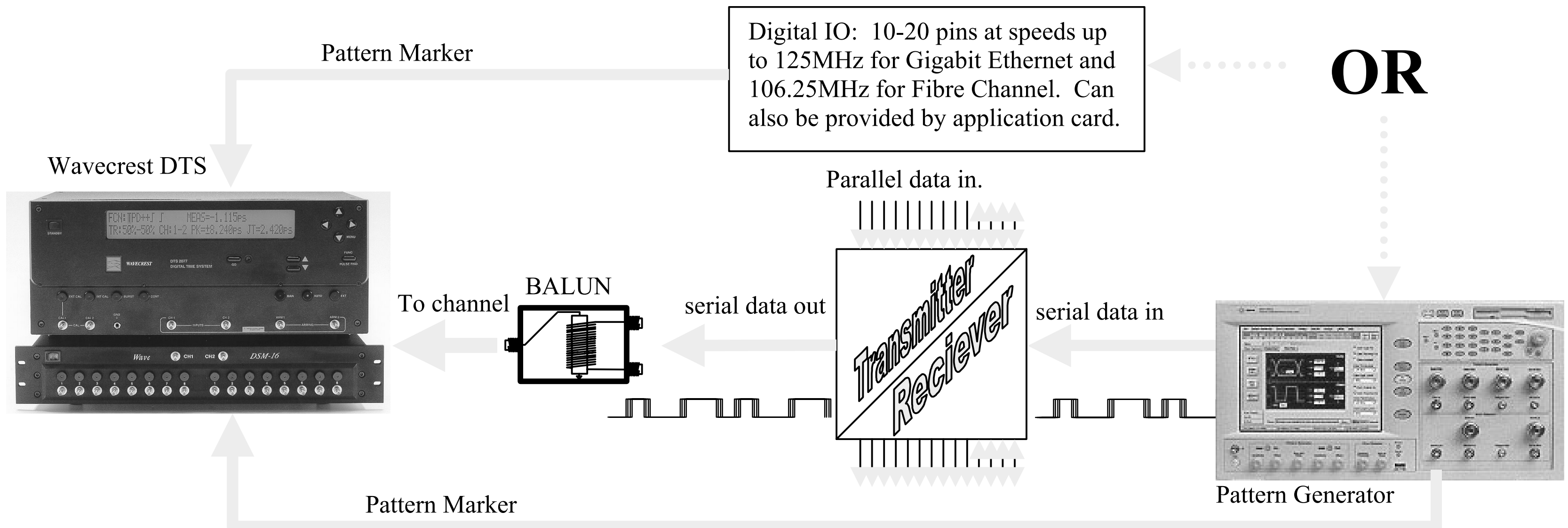


2 histograms of Δt measurements. One for rising edges, one for falling edges.

- Selecting the "real" measurements
  - The tool automatically eliminates any time measurements which exceed one bit period (just as the scope does)
  - Be careful when correlating with o'scope. Most o'scopes have a trigger delay that forces the user to look at the wrong data histogram.
- Skew of histograms indicates asymmetric cross point.
  - Rising Edge Histogram before Falling Edge Histogram indicates cross point is below starting trigger level.
  - Falling Edge Histogram before Rising Edge Histogram indicates cross point is above starting trigger level

(Eye Histogram is basically a T_{PD} measurement with built in data filters.)

Jitter Measurements on ONLY data

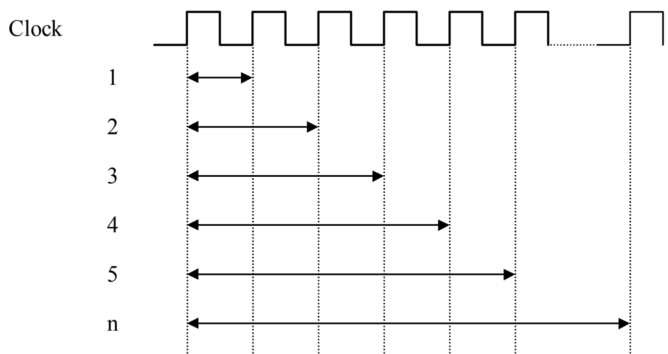


- Use Pattern Marker to optimize data dependant jitter separation.
  - Optimal accuracy is achieved when using pattern marker and TailFit™ on short patterns
- Use Balun and 50% Voltage level
- Data Plots include:
  - Data Dependant Jitter vs. UI (for pattern sensitivity testing)
  - Uncorrelated Jitter vs. frequency (for PJ detection)
  - Bathtub Curve (Eye Closure vs. BER)
- Based on patented Accumulated Time Analysis™ routine

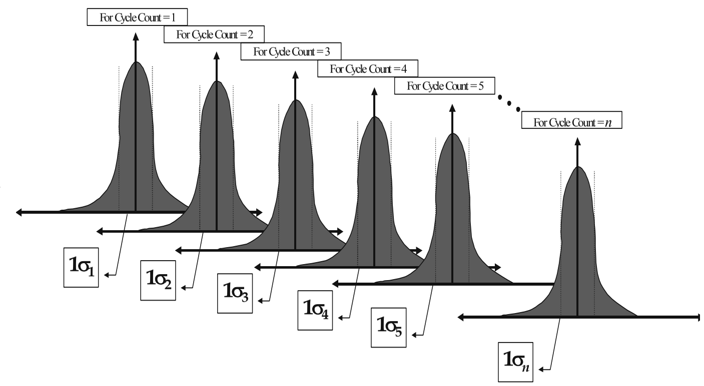
The Math Behind VISI dataCOM Tools

Review of Accumulated Time Analysis™

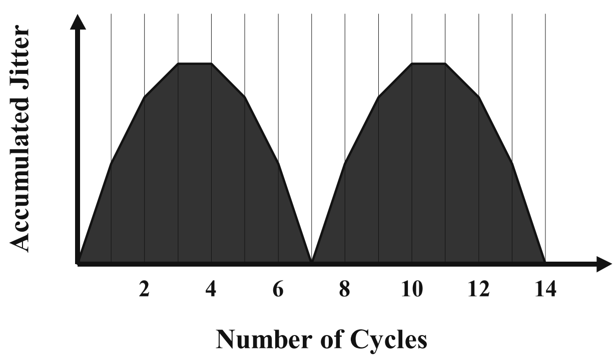
Measurement Schedule



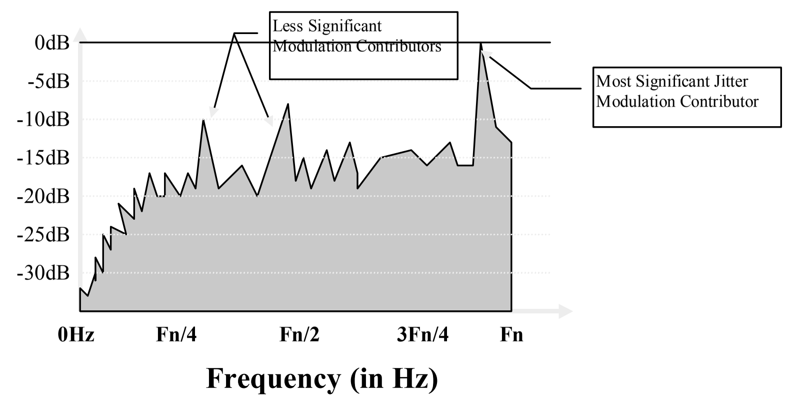
Distribution of Time Measurements



Jitter Analysis Graph with Period as Function

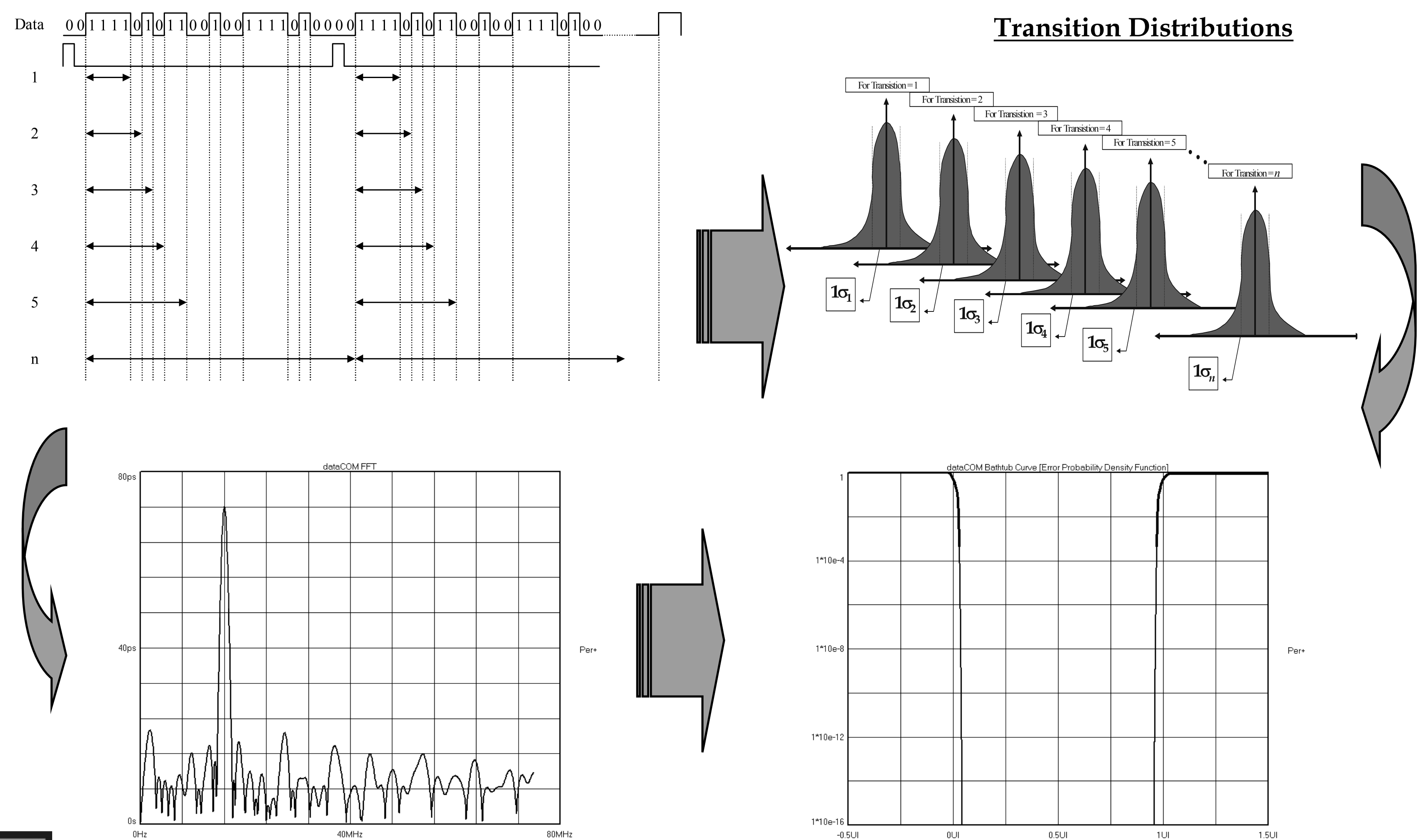


FFT of Accumulated Jitter Data



Fn = Apparent Nyquest Frequency

VI™ DataCOM Known Pattern & Pattern Marker - Theory of Operation

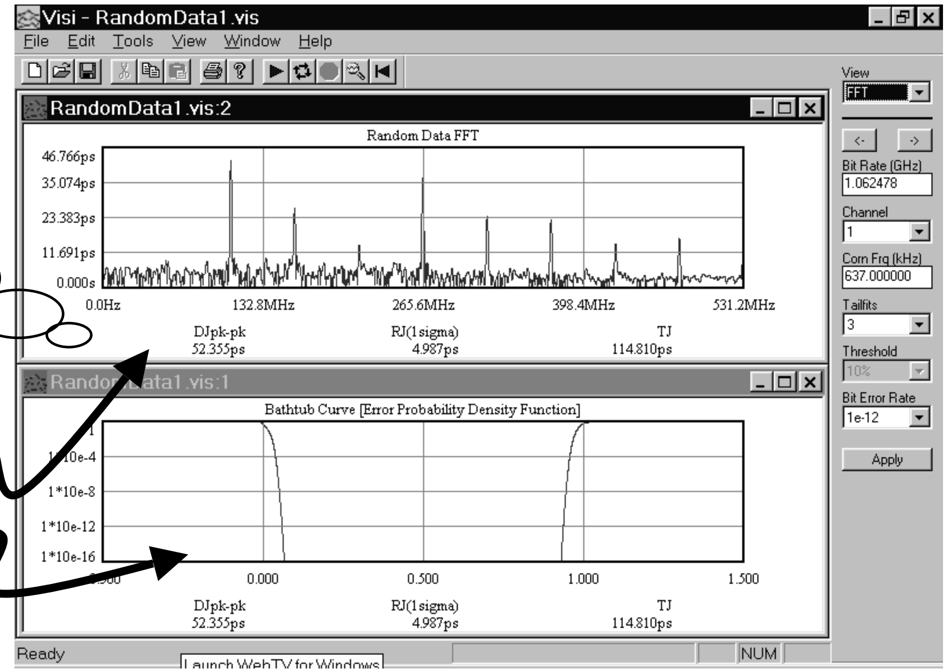


How do I Generate a Marker?

- Using Wavecrest's AG100
  - Recover bit clock and perform pattern recognition for use with patterns with a header section preceding it
  - Count bit clock for pattern length trigger for patterns with constant length. (no random idles interleaved.)
    - User can program the length of the pattern or the bit stream to trigger on
  - Built in Balun
  - Built in linear amplifiers for low swing signals

Random Data Tool

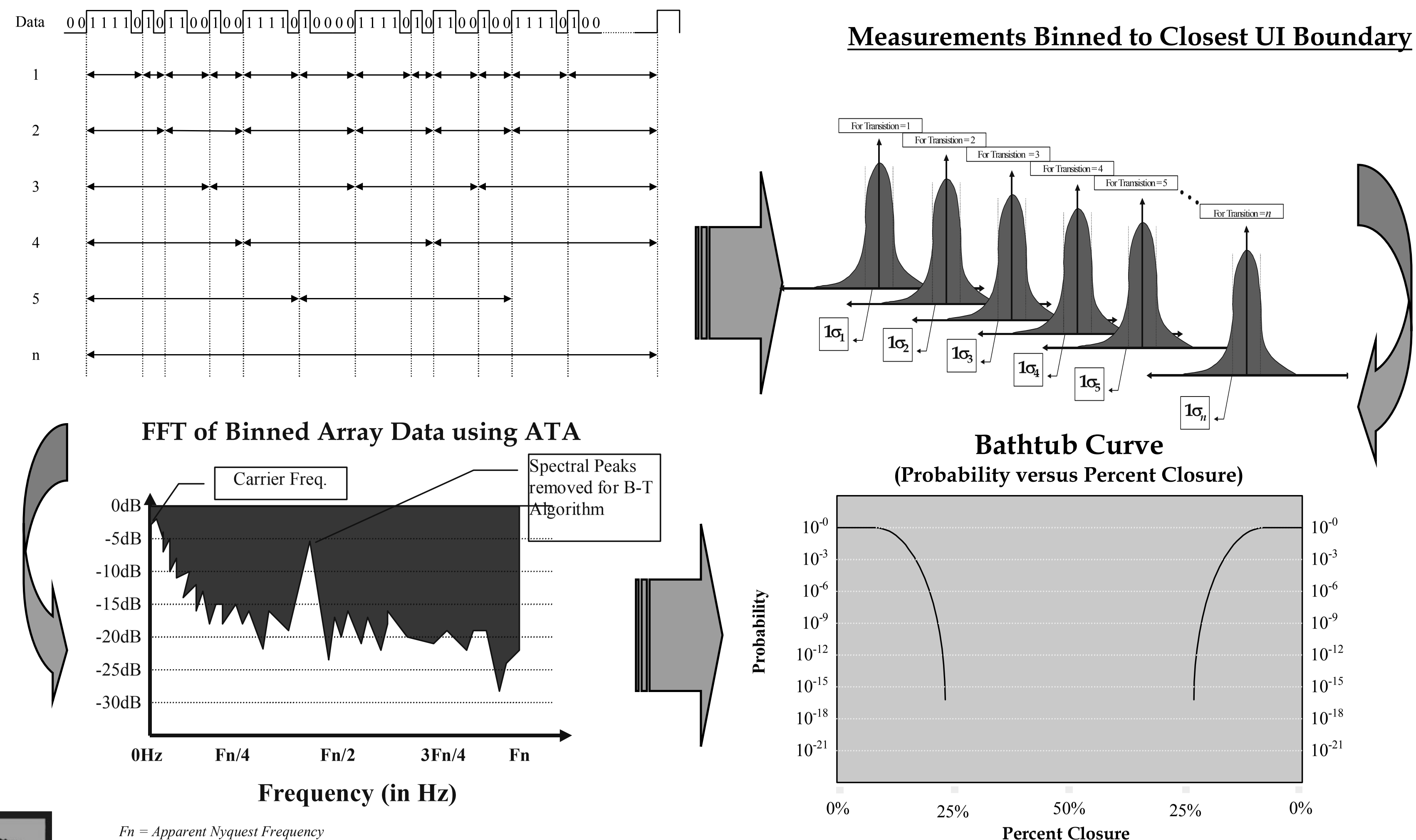
This is the first tool featuring User Friendly Controls. Watch for VISI 6.0 which will feature this capability in all tools!



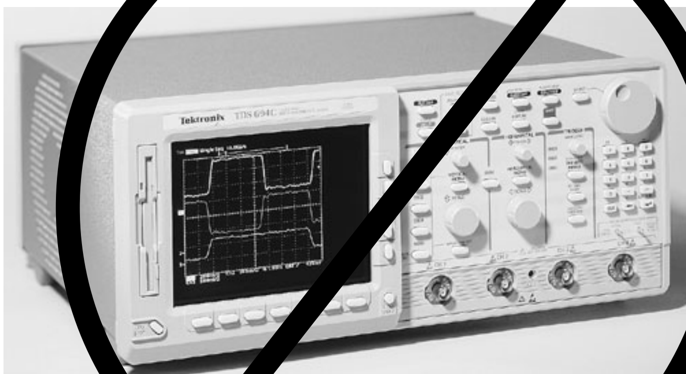
Jitter Frequency Plot and Bathtub Curve all without any knowledge of the pattern

- Based on random data streams, Random Data Tool lets the user analyze any data stream with no marker, bit clock nor knowledge of the pattern.
- Uses TailFit™ algorithm and special sampling technique to look at fully random data streams.

VI™ DataCOM Random Pattern Theory of Operation

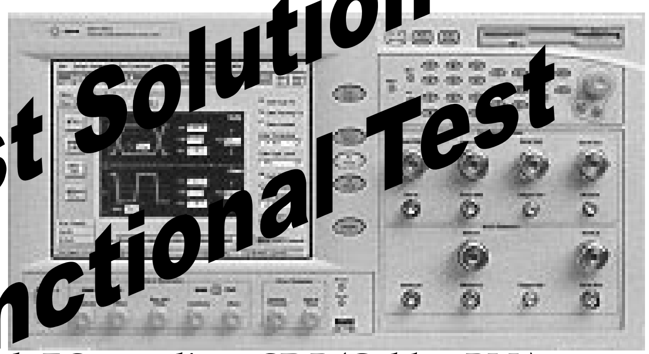


Jitter Output Testing



Cann… us… a Digitizing Oscillosco…

Best Solution for Jitter Analysis



Best Solution for Functional Test

(with FC compliant CDR(Golden PLL) for triggering)

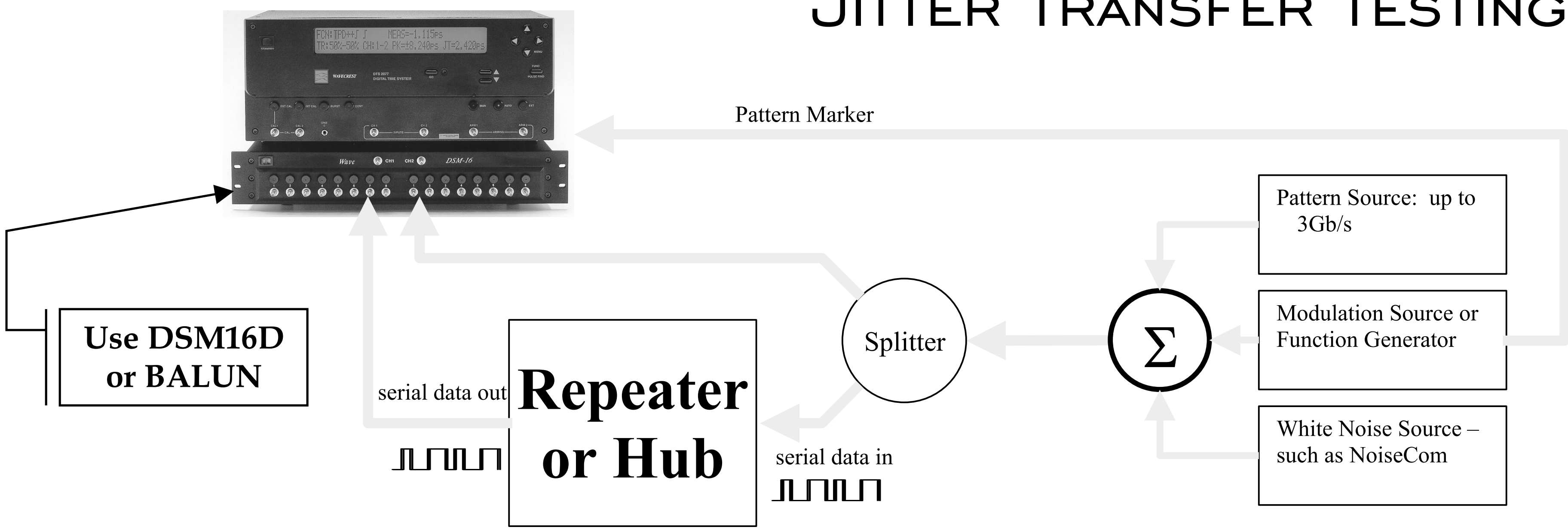
Best Solution for Waveform Analysis

(with FC compliant CDR(Golden PLL) for triggering)

Jitter Transfer Testing

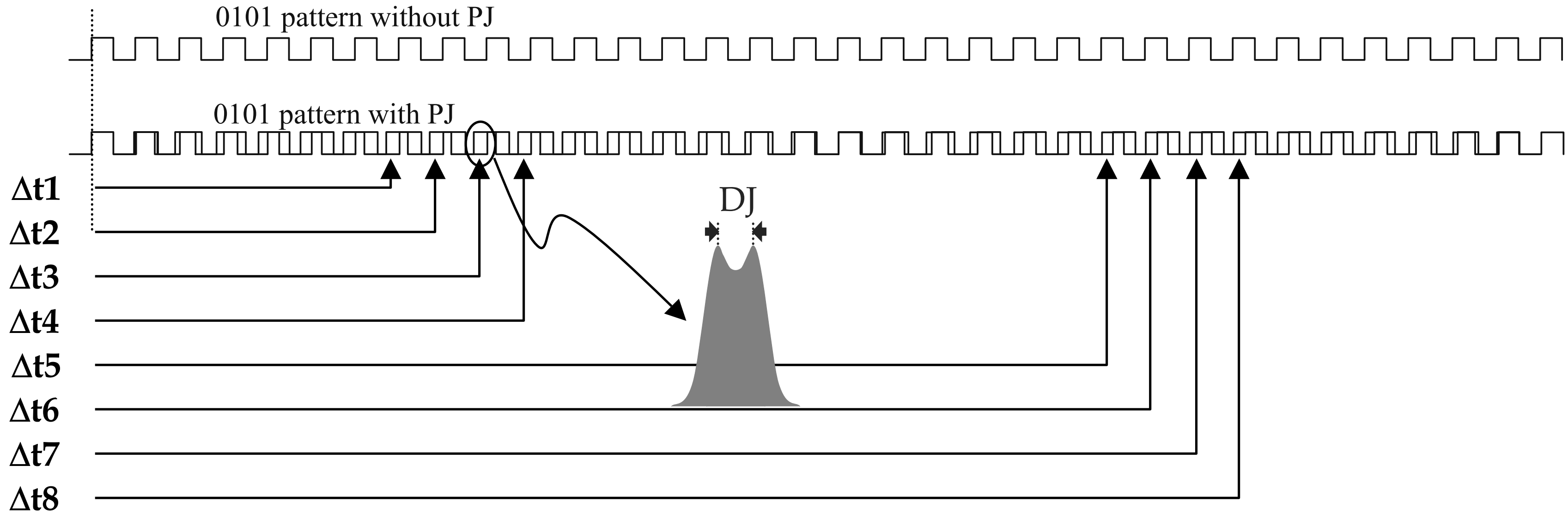
These are some helpful hints based on real world experiences from SONET testing. As you may know, Jitter Transfer has not yet been addressed by the MJS committee. These suggestions are included to provide insight into techniques for measuring Jitter Transfer with the Wavecrest Communication Signal Analyzers. Obviously, Other tools, such as SONET analyzers, already have this capability although their measurement time is quite long. Also, Wavecrest is continuing to develop solutions that improve ease of use.

Jitter Transfer Testing



- Use Pattern Marker when analyzing data.
  - Can also use clock stream in which case, no pattern marker is necessary.
- Use BALUN or DSM16D for differential signal support.
  - DSM16D is a 4GHz Bandwidth, 8D:2SE matrix.
- Signal summation could be done with matched dividers or through internal power summation of instrumentation.
  - Some models of pattern generator and noise source have signal inputs which can be used to sum signals.
- Use DTS to analyze the input signal to adjust Noise and Modulation source to desired amplitude.
- Noise Source not necessary for SONET Jitter Transfer testing.

Measuring Jitter Transfer

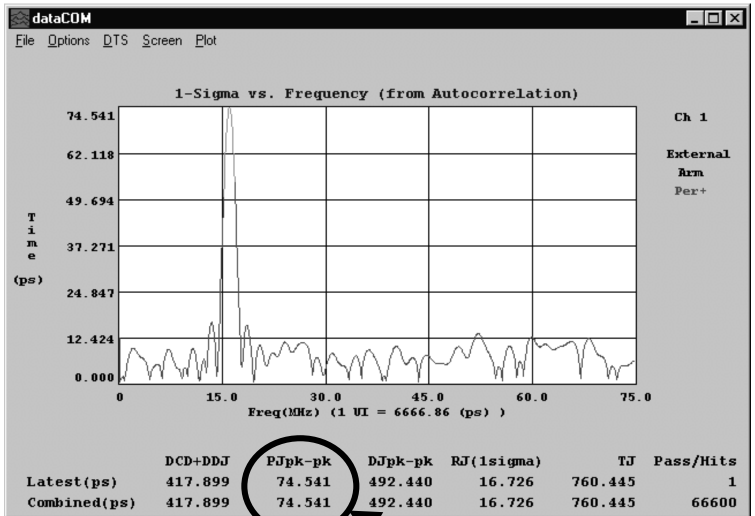


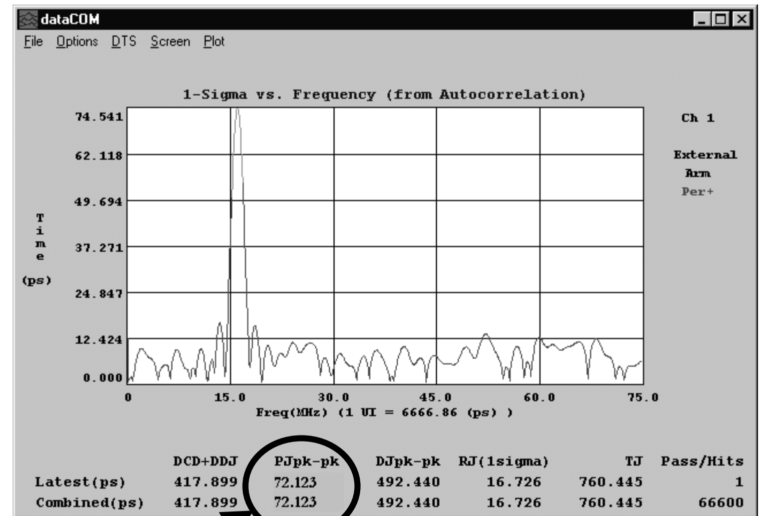
- Measure elapsed time and analyze the jitter for accumulated periods of [FC/(2*FM) ±2]
  - The "±2" is to account for inaccuracy of modulation source
- Find the maximum DJ for Δt1-4 and Δt5-8. Average the max values. (can also use pk-pk of the distribution for faster results)
  - Two groups are used to account for measurement repeatability.
- Then, compare the DJ going into the device to the DJ coming out using the gain equation:

$$\text{Gain} = 20 \log(DJ_{OUT}/DJ_{IN})$$

- Perform this test for several frequencies.

Using VISI for Jitter Transfer

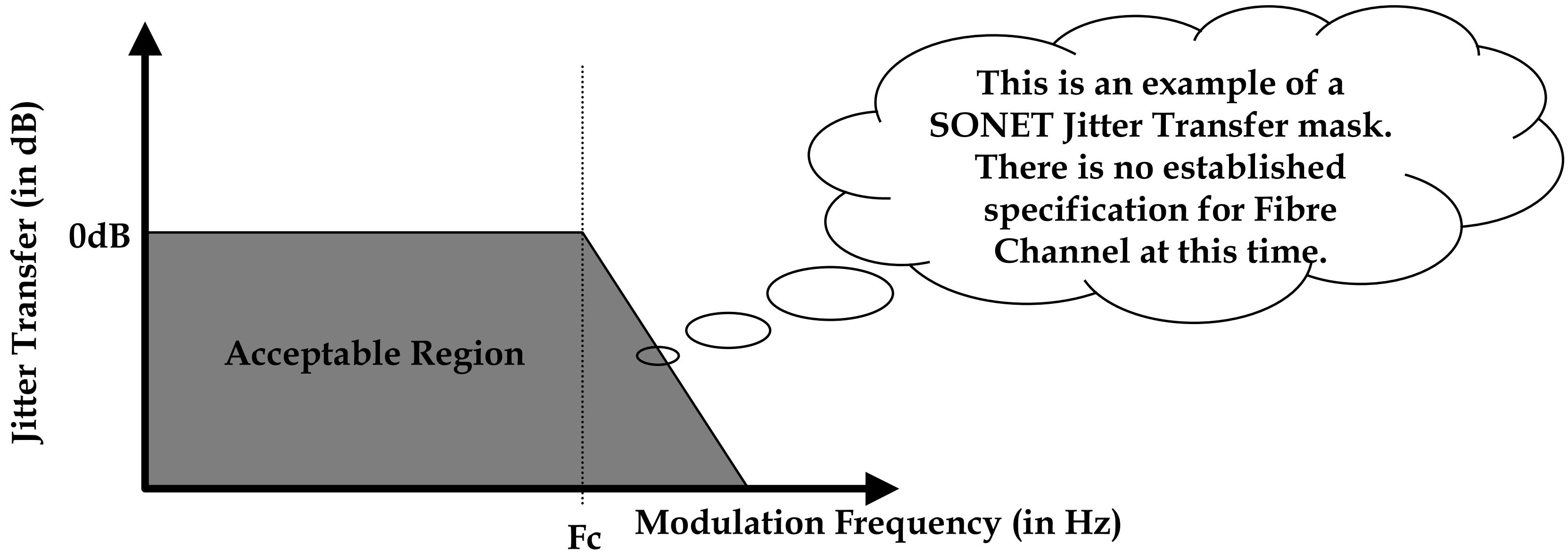




Compare these two numbers with Gain Equation

- Using VISI, measure $PJ_{PK\text{-}PK}$ on the input and the output of the device of system.
- Use this technique for analyzing Jitter Transfer on data streams or clock-like patterns.
- Can also be done in GPIB commands for automated laboratory programming environments (LABVIEW).

Jitter Transfer Specifications

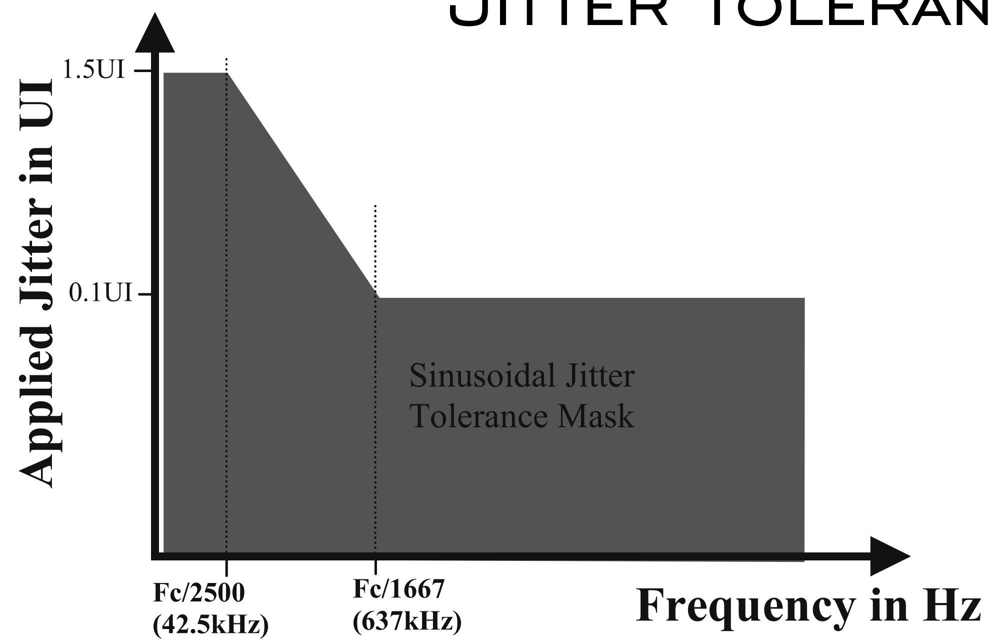


JITTER TRANFER –

The ratio between the jitter output and jitter input for a component, device, or system often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter. A zero dB jitter transfer indicates the element had no effect on jitter. The ratio should be applied separately to deterministic jitter components and Gaussian (random) jitter components. The concept of jitter transfer is not addressed in [MJS] document.

Jitter Tolerance Testing

Jitter Tolerance Testing



- Jitter Tolerance on Fibre Channel devices consists of applying prescribed amounts of non-sinusoidal DJ and RJ in conjunction a frequency sweep of sinusoidal jitter
  - Applying all components simultaneously tests the interaction of each jitter component.
  - Be sure to apply the correct amount for the given compliance point.h

Jitter Tolerance Specification

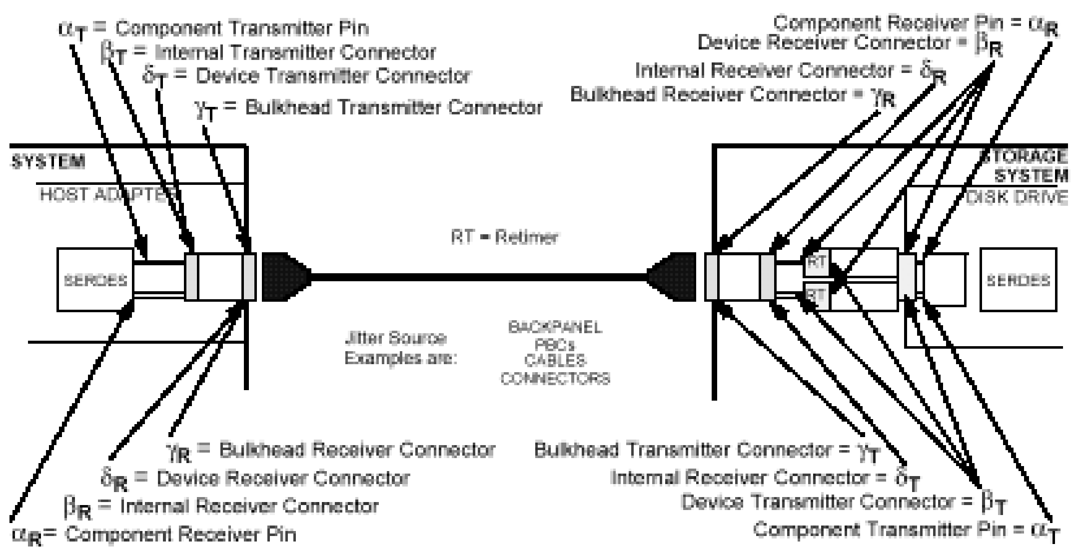
Table 7 – 1,0625 GBaud jitter tolerance allocation example

Variant	Jitter (Unit Interval - UI)								
	Component	α_T	β_T	δ_T	γ_T	γ_R	δ_R	β_R	α_R
100-SM-xx-x (single mode)	DJ Sinusoidal Total	0,10 0,10 0,31	0,11 0,10 0,28	0,12 0,10 0,30	0,21 0,10 0,48	0,23 0,10 0,52	0,36 0,10 0,66	0,37 0,10 0,68	0,38 0,10 0,70
100-Mx-xx-x (multi-mode)	DJ Sinusoidal Total	0,10 0,10 0,31	0,11 0,10 0,28	0,12 0,10 0,30	0,21 0,10 0,48	0,24 0,10 0,52	0,36 0,10 0,66	0,37 0,10 0,68	0,38 0,10 0,70
100-xx-EL-x (copper)	DJ Sinusoidal Total	0,10 0,10 0,31	0,11 0,10 0,33	0,12 0,10 0,35	0,13 0,10 0,37	0,35 0,10 0,64	0,36 0,10 0,66	0,37 0,10 0,68	0,38 0,10 0,70

1. Note that the sinusoidal component of 0,10 UI is valid for frequencies of 637 kHz and higher. For frequencies below 637 kHz, the magnitude of the sinusoidal component must meet figure 9.
2. Although the jitter output corner frequency and jitter tolerance frequency maybe the same as detailed in this recommendation, it is recommended that the jitter tolerance corner frequency be greater than the jitter output corner frequency.
3. α_T, β_T, δ_T and γ_T are included to indicate that the jitter test signal can be injected at any point in the system to test the α_R point's jitter tolerance.

This implies a total RJ component .22UI or .0157UI (1σ)

α_R is made at the component of the receiver.



MJS Recommended Setup

Use the DTS to verify the amplitude of the jitter components being applied.

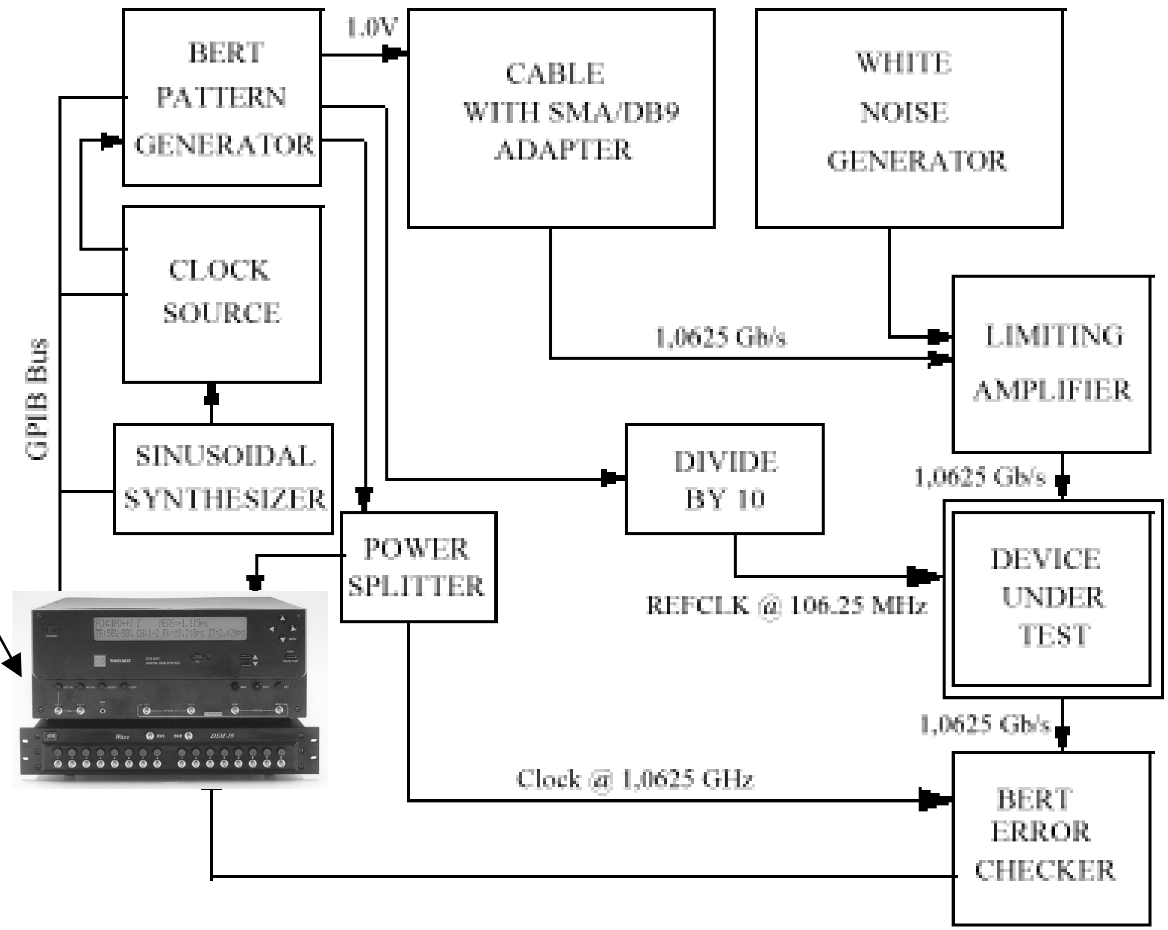
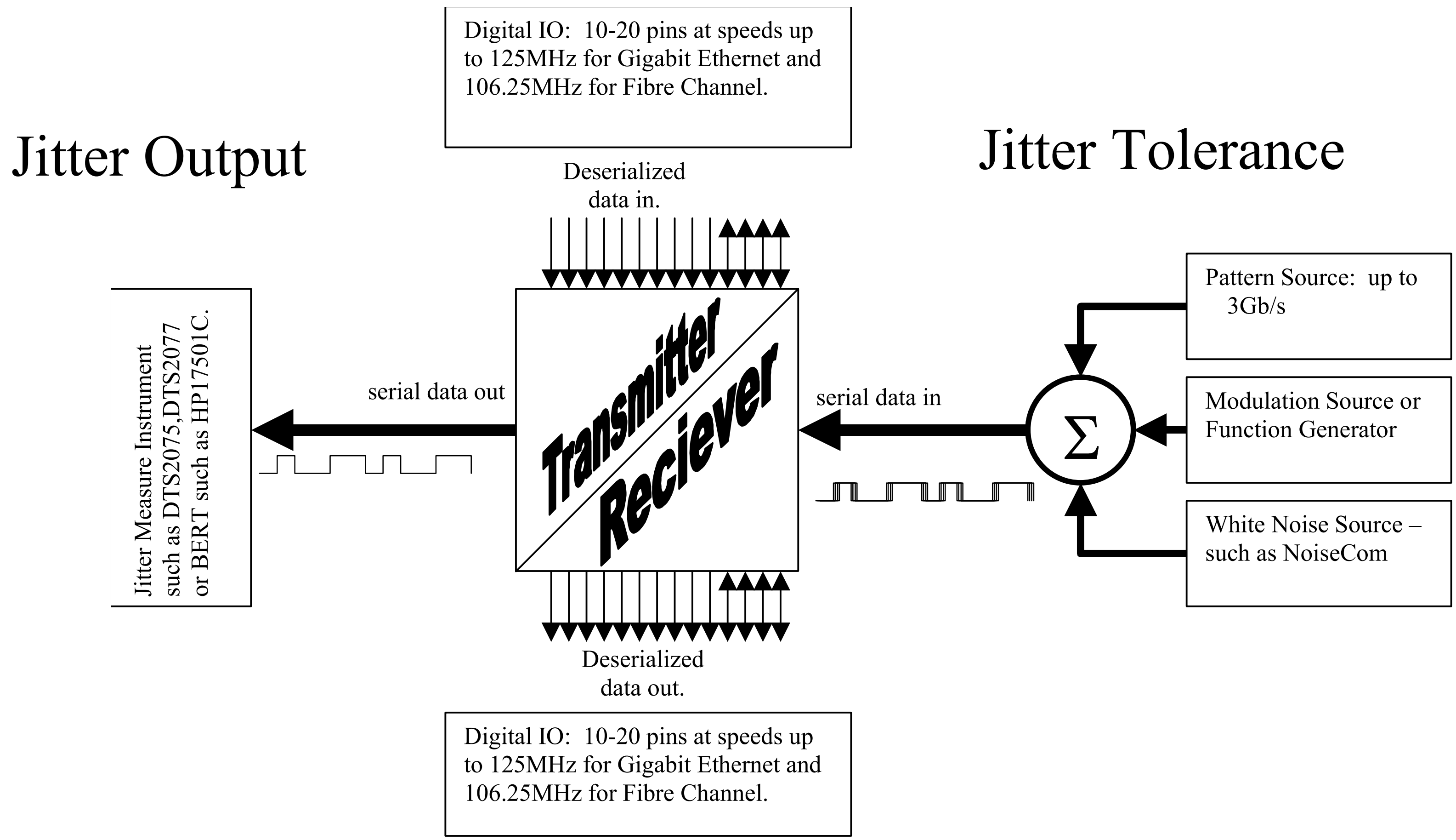
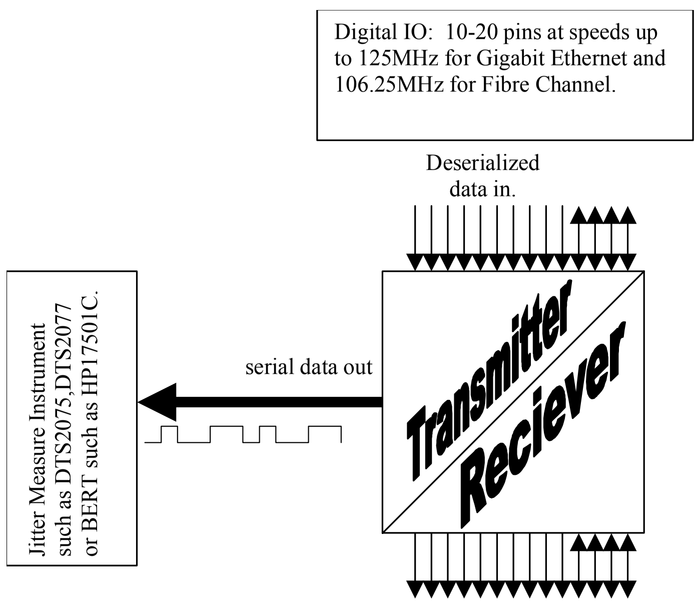


Figure C.4 – Example of Jitter Test Setup for 10-bit SerDes

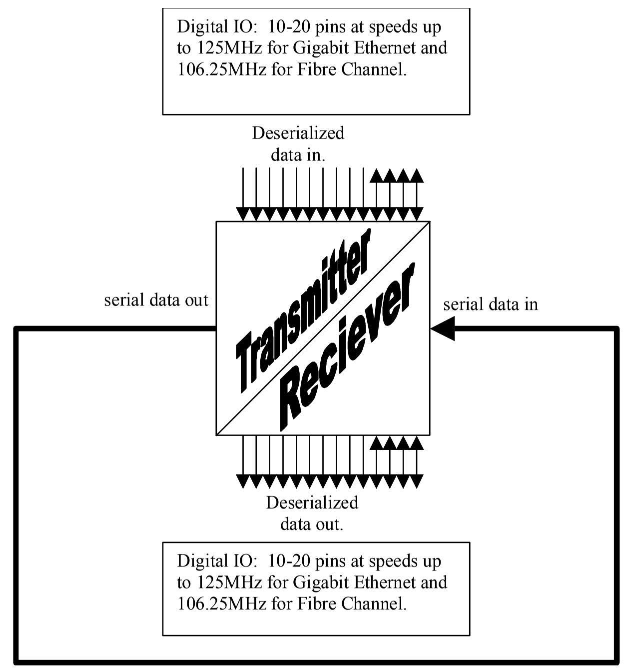
Fibre Channel and Gigabit Ethernet Complete Jitter Testing



Fibre Channel and Gigabit Ethernet Simplified Jitter Testing



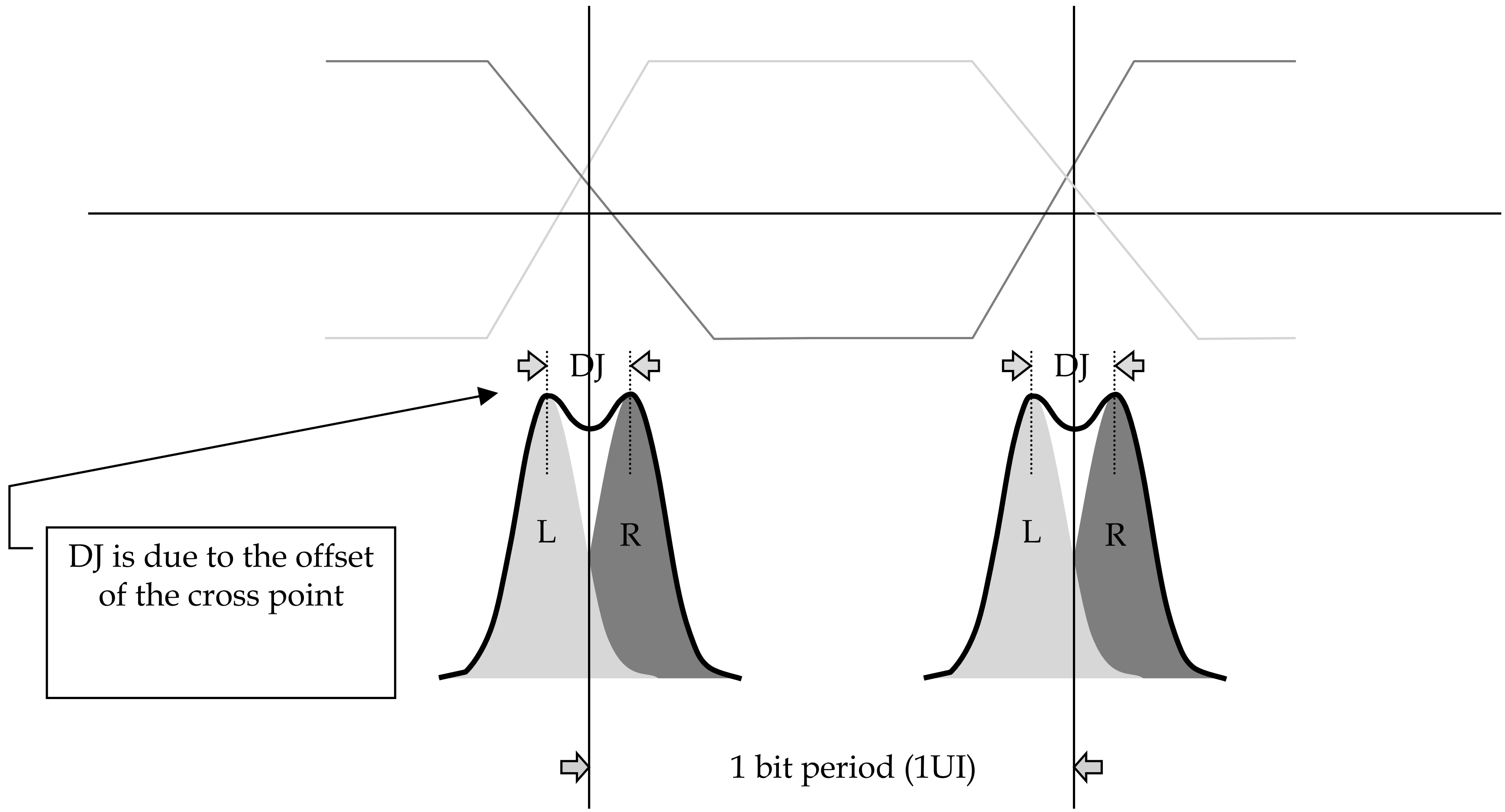
Jitter Output



Receiver Port Testing

Proper Measurement Techniques – Jitter Output (Generation)

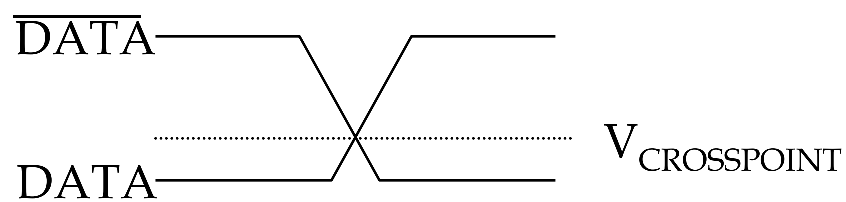
WHERE SHOULD I TRIGGER THE MEASUREMENT?



- You must measure at the 50% point and you must use a BALUN.
- The 50% point is indicative of the point in time when the two complimentary signals are equal in voltage and thus best represents the point at which the differential receiver switches.

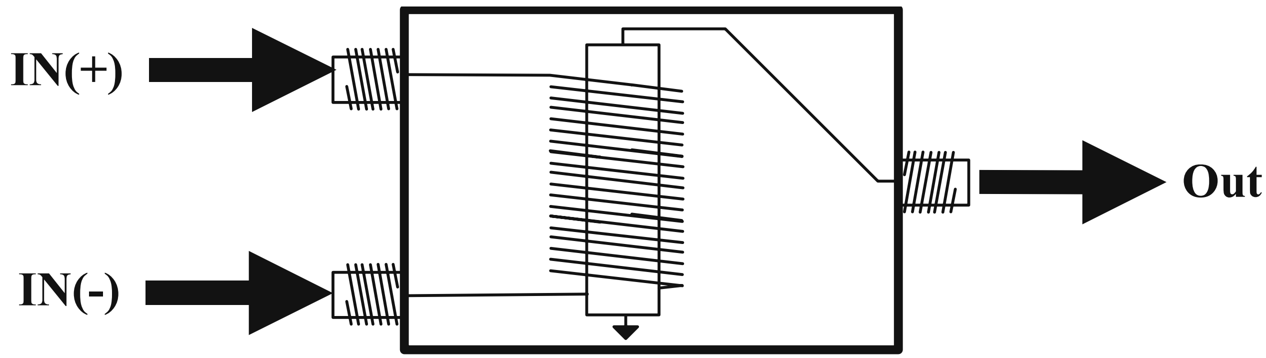
Measuring Differential Signals

- High Frequency Differential Signals Need Special Attention
  - Rise time and fall time for a given device are typically not equal.
  - Differential Input pins (receivers) typically transition when the two complimentary signals are transitioning through the same voltage. This voltage is called the crosspoint voltage and is depicted here.



- Jitter Measurements and Propagation Delay measurements must be taken from the crosspoint reference.
  - Since Differential Input pins use the crosspoint as the transition indicator, it is imperative that all time measurements be made from this point.
  - This is best done by using a balun

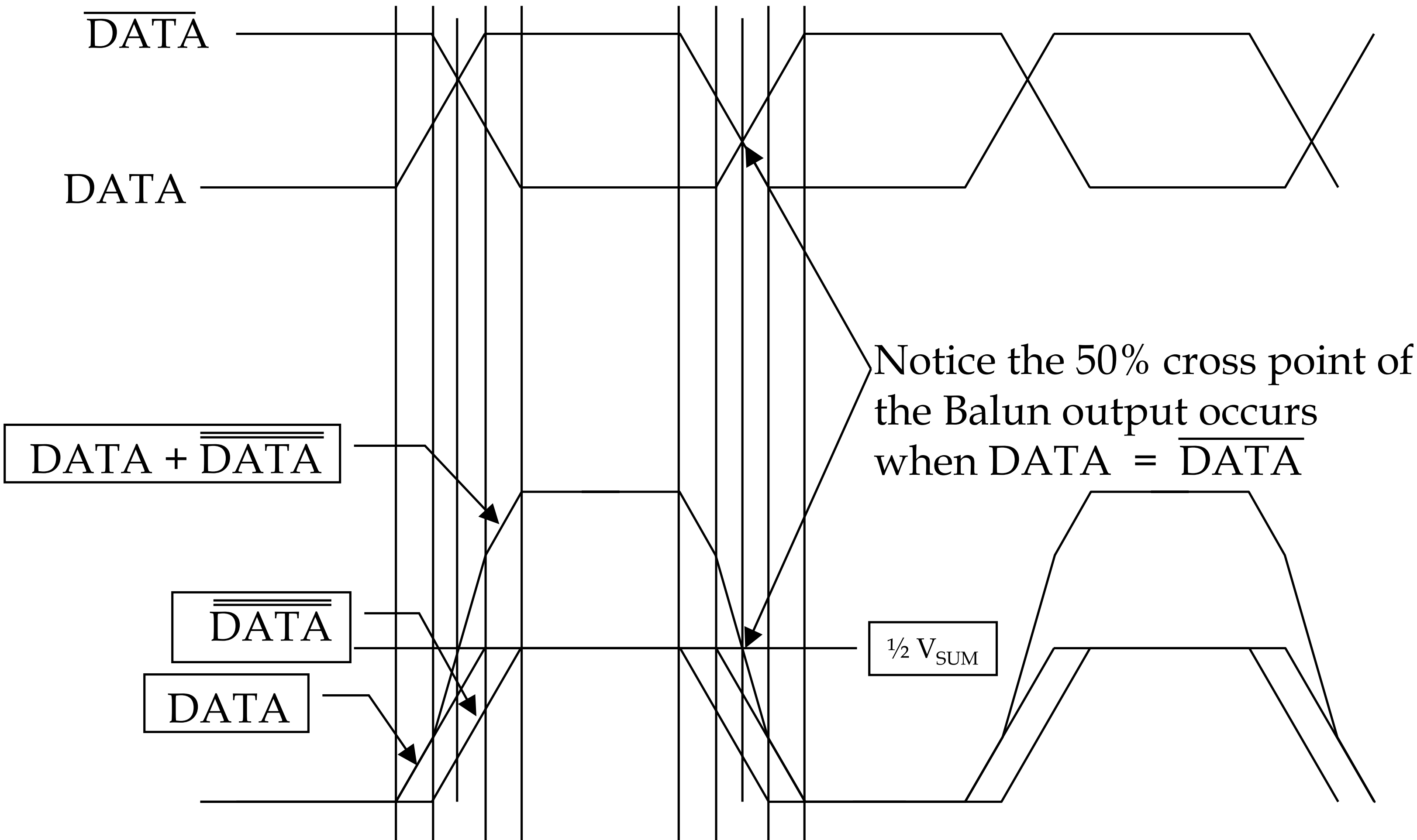
What is a Balun?



- Balanced to Unbalanced Converter (BALUN)
  - Used to convert differential signals to single ended using linear components.
  - Uses simple wound core architecture to convert differential signal single ended.
  - The output of the BALUN is AC coupled.
  - Permits high performance time measurements to be made by generating a single ended signal that has the same timing criteria as the original differential stimulus.
  - Single ended signal is a mathematical equivalent to:

$$\text{Out} = \text{IN}(+) - \text{IN}(-)$$

Understanding Balun Devices



Wrap-up

- Jitter Components are best analyzed with Jitter Tools
  - Must be able to separate RJ, PJ and DDJ
  - Must be able to quantify the amplitude and frequency of the jitter
- Every Tool has it's place
  - Use BERT for functionality testing
  - Use Scope for waveform verification
  - Use Wavecrest DTS for timing and jitter analysis
- Be sure to visit our web page for the latest material concerning Communication Signal Analysis

www. Wavecrest.com

- Questions?

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